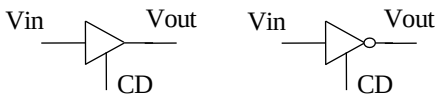
## Buffers

- Single gate often has to drive a large fan-out. Large on chip load (pF order) are
  - busses
  - clock network
  - control wires
  - in memories: many storage cells are connected to few control and data wires
- Worst case occurs when gate drive off-chip load (20-50 pF)
  - pad capacitance
  - package wiring
  - circuit board wiring



- The increase in the load capacitance proportionally increases the propagation delay
- A buffer circuit is used to maintain the speed performance of the circuit
  - buffering with a single inverter
  - buffering with multiple inverter

## Buffer Tri-State




- When one device is sending data on a bus, all other sending devices should be disconnected

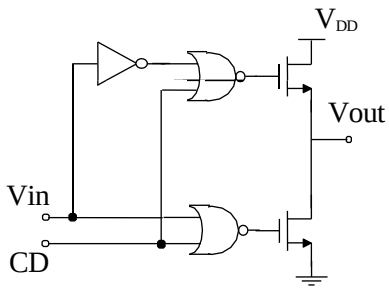
⇩

*The other device must be put in High-impedance state Z*

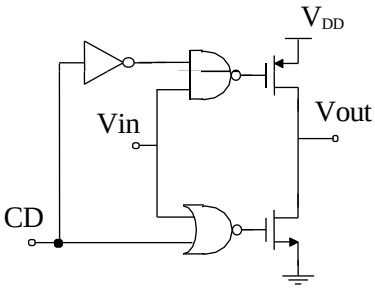
- The output of this kind of device is 1,0 and Z *tri-state* buffer



## Tri-State NMOS

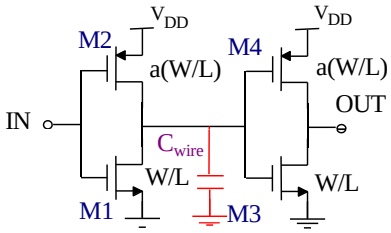



## Tri-State CMOS




- CD = 1 switch off all output transistors

## Cascade of equal inverter




- If an inverter is loaded with another inverter ratio of N and P aspect ratio is different than $\mu_n/\mu_p$

$$C_{eq}=C_{wire}+C_{DB1}+C_{DB2}+2(C_{GD1}+C_{GD2}+C_{GD3}+C_{GD4})+C_{GS3}+C_{GS4}$$

$$\Downarrow$$

$$C_{eq}=C_{wire}+C_{DBn}+C_{DBp}+4(C_{GDn}+C_{GDp})+C_{GSn}+C_{GSp}$$



$$\frac{(W/L)_p}{(W/L)_n}=a \quad [W_p=a\,W_n] \quad \Rightarrow \quad C_{eq}=C_{wire}+(1+a)(C_{DBn}+4C_{GDn}+C_{GSn})$$

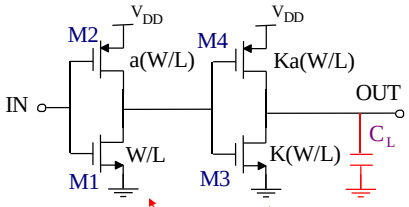
$$=C_{wire}+(1+a)C'$$

$$\tau_{PD}=\frac{\tau_{LH}+\tau_{HL}}{2}\cong\frac{C_{eq}}{2}V_{DD}\left(\frac{1}{\beta_n(V_{DD}-V_{tn})^2}+\frac{1}{\beta_p(V_{DD}+V_{tp})^2}\right)=$$

$$=\frac{C_{wire}+(1+a)C'}{2}\left(1+\frac{\mu_n}{a\mu_p}\right)\frac{V_{DD}}{\beta_n(V_{DD}-V_{tn})^2}$$

$$\frac{d}{da}\tau_{PD}=0 \quad \Rightarrow \quad a=\sqrt{\left(1+\frac{C_{wire}}{C'}\right)\frac{\mu_n}{\mu_P}}$$

## A single inverter as buffer




*$\tau_{PD}$ of a minimum size inverter loaded with a minimum inverter*

$$\tau_{PD} = \tau_{PDinv} + \tau_{PDbuf} = K\tau_{PDo} + \frac{C_L}{C''}\frac{1}{K}\tau_{PDo}$$

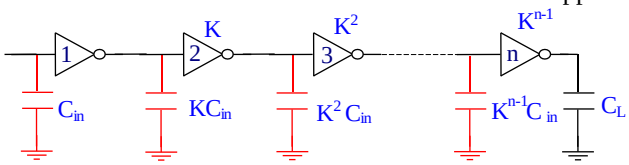
$$C'' = (1+a)C_{DBno} + 4(1+a)C_{GDno} + (1+a)C_{GSno} \approx (1+a)C'$$

$$\frac{d}{dK}\tau_{PD} = 0 \Rightarrow K_{opt} = \sqrt{\frac{C_L}{C''}}; \quad \tau_{PDopt} = \sqrt{\frac{C_L}{C''}}\tau_{PDo}$$



## Tapered buffer

Academic approach (1975)




- Each stage is scaled up with a constant factor *K*

each stage has an equal propagation delay

- To achieve the same delay for the last stage $K^n = \frac{C_L}{C_{in}}$

$$n = \frac{\ln(C_L / C_{in})}{\ln(K)}$$

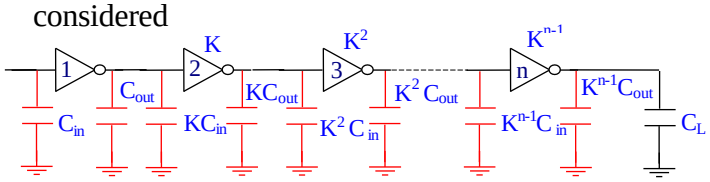
$$\tau_{PDtot} = \sum_{i=1}^{n} \tau_{PDi} = nK\tau_{PDmin} = \frac{K}{\ln(K)} \tau_{PDmin} \ln\left(\frac{C_L}{C_{in}}\right)$$

$$\frac{d}{dK} P_{Dtot} = 0 \quad \Rightarrow \quad \ln(K) - 1 = 0$$

$$K \sim e \sim 2.72$$

$$n = \ln\left(\frac{C_L}{C_{in}}\right)$$

- The output capacitance of each stage should be considered






- By using more precise transistor model which takes into account small channel effects (Trans. on VLSI March 95)

$$\frac{C_L}{C_{in}} \cong 10 \Rightarrow n = 2 \qquad \frac{C_L}{C_{in}} \cong 1000 \Rightarrow n = 5$$

- The design can take into account other constraint such as power dissipation, area, reliability
  - the power dissipation decrease decreasing N
  - the reliability (very low for N=2) increase with N

$$\begin{aligned} 10 \le C_L / C_{in} \le 100 &\Rightarrow 2 \le N \le 3 \\ 100 \le C_L / C_{in} \le 1000 &\Rightarrow 3 \le N \le 4 \\ 1000 \le C_L / C_{in} \le 10000 &\Rightarrow 4 \le N \le 5 \end{aligned}$$