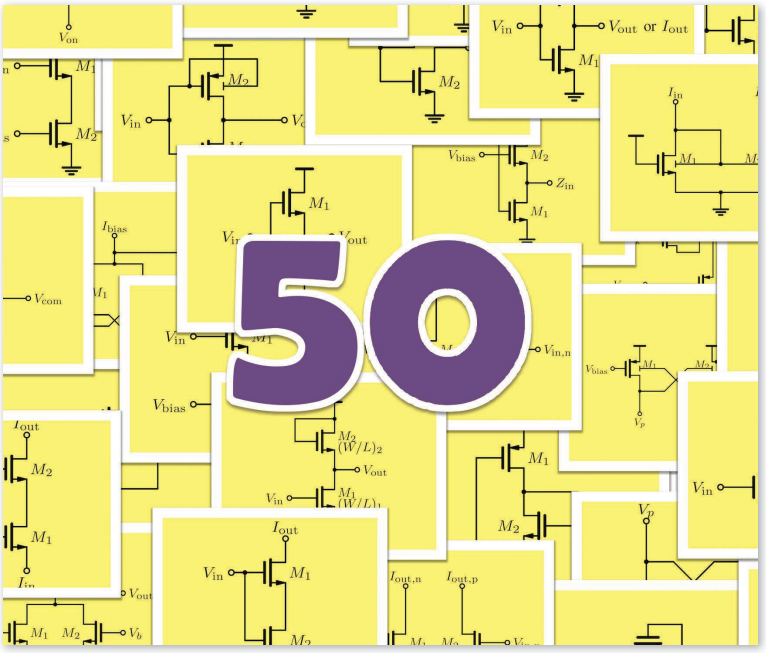
Harald Pretl and Matthias Eberlein

Fifty Nifty Variations of Two-Transistor Circuits



EHRENTRAUD HAGER

A tribute to the versatility of MOSFETs

We present a compendium of two-metal-oxide-semiconductor (MOS)-transistor circuits, which span the range from simple standard configurations to ingenious arrangements. Using these building blocks, circuit designers can assemble a vast array of complex analog functions. This (incomplete) collection shall serve as a reference and inspiration to junior circuit designers and hopefully contains at least one unexpected example for professional engineers.

Overview

Analog circuit design is wonderfully creative. The MOS field-effect transistor (MOSFET) is an exceptionally versatile device, operating as a switch, current source, resistor, diode, and capacitor, depending on bias conditions. For fun and to demonstrate the sheer infinite possibilities in circuit design using MOSFET, we present a collection of simple (and sophisticated) circuits that employ two transistors (not counting fixed-bias and supply voltages and fixed-bias currents). Often, circuit designers construct complex circuits from these basic building blocks.

This compendium is a tribute to all of the ingenious minds out there and the circuit design giants on whose shoulders we are standing today. This sample of practical two-transistor circuits, to the best of the authors' knowledge, contains beneficial and often-used configurations. A few circuits are of a more curious and academic nature; they might lack power-supply rejection or show other deficiencies, and some circuits use the body connection as active terminals, which might not be feasible in some CMOS technologies. Generally, one has to be aware of the body effect and its impact.

Many more two-transistor circuits are yet to be discovered. An exhaustive search of graphs using one or two voltage-controlled current sources (which are well-approximated by MOSFET) resulted in 150 potentially useful circuits [1]. One of them was identified as a valuable new amplifier configuration [2]. By pushing this idea further, a study identified 582 possible circuit topologies using two transistors. Repeating this exercise using three transistors, a whopping 56,280 elementary configurations have been found [3].

To keep our overview reasonable, we do not include complementary

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circuits that can be constructed by swapping n-MOSFET (NMOS) for p-MOSFET (PMOS) devices (or vice versa).

Logic Circuits

First, we present simple circuits that operate on logical inputs, like the inverter (Figure 1), and an improved low-voltage version that exploits the body terminals in a DTMOS inverter (Figure 2). Terminating an unused input of a logic gate to a logical one or zero, an ESD-safe tie-zero or tie-one, respectively, should be utilized, like the one presented in Figure 3. Using the unusual arrangement in Figure 4, we can implement an XNOR logic function while the implementations of NAND and NOR as presented in Figures 5 and 6, respectively, are the fundamental building blocks of the digital universe.

Basic Circuits

This section presents the basic circuits constituting the fundamental building blocks of the analog and mixed-signal world, like the current mirror displayed in Figure 7. The differential pair (Figure 8) is constructed alternatively with or without a tail current source, which is often called a *pseudodifferential pair*. The source follower in Figure 9 is one

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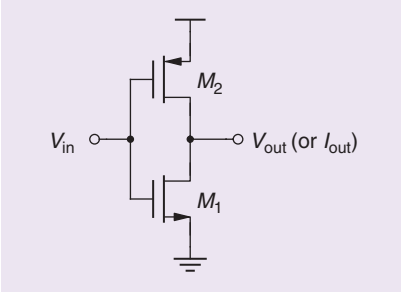

FIGURE 1: The ubiquitous digital inverter. The input voltage V_{in} switches one of the transistors on while the other is off [4].

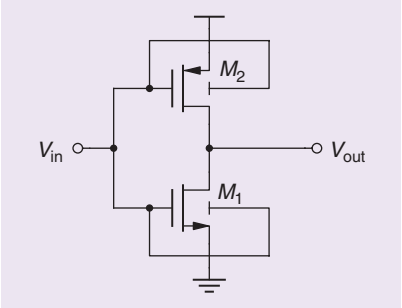

FIGURE 2: The dynamic-threshold-voltage MOSFET (DTMOS) inverter achieves an improved current drive at low-leakage current. It needs to be operated at low supply voltages to avoid a forward bias of the well diodes [5].

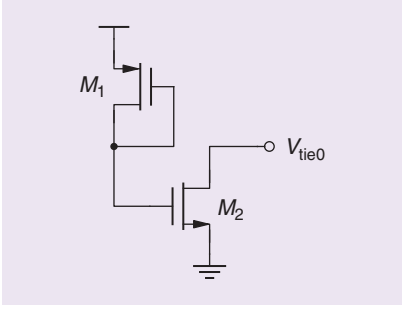

FIGURE 3: An electrostatic discharge (ESD)-safe tie-zero for unused CMOS logic inputs (no MOSFET gate is tied directly to a supply rail). The tie-one can be constructed accordingly.

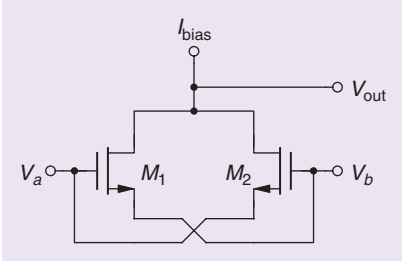

FIGURE 4: Using a current source I_{bias} with finite output impedance to bias this structure, this circuit implements an XNOR logic function ($V_{out} = \overline{V_a \oplus V_b}$). The logic inputs V_a and V_b must be driven by low-ohmic logic levels between V_{DD} and V_{SS} [6].

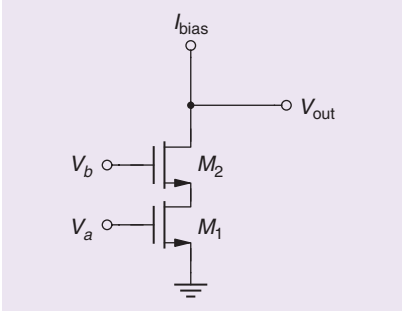

FIGURE 5: This series connection of two MOSFETs realizes a logical NAND function ($V_{out} = \overline{V_a \wedge V_b}$).

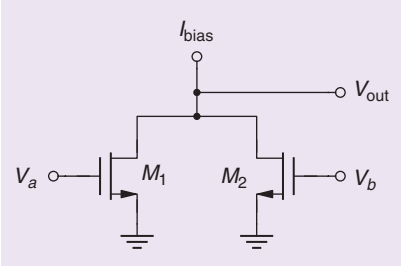

FIGURE 6: This circuit complements the logic gates implemented in Figures 4 and 5 and realizes a NOR function ($V_{out} = \overline{V_a \vee V_b}$).

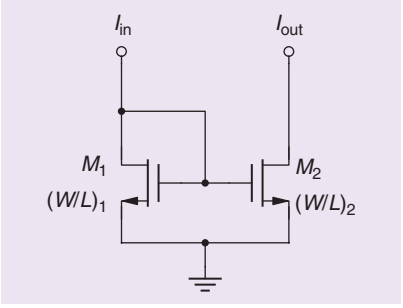

FIGURE 7: The basic current mirror achieves a simultaneous copying and sizing of $I_{out} = (W/L)_2/(W/L)_1 \cdot I_{in}$ according to the dimensions of M_1 and M_2 [7].

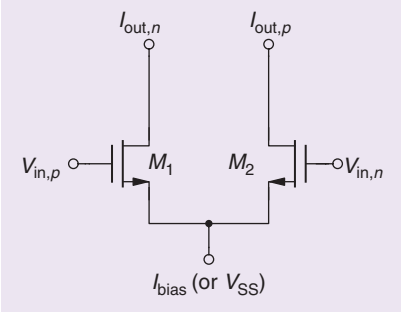

FIGURE 8: The ubiquitous differential pair, like the current mirror in Figure 7, is a fundamental building block in integrated circuits [8]. The pseudodifferential variant spares the tail current source's headroom in exchange for reduced common-mode rejection but with the benefit of class-AB action.

The generation of a bias voltage is a task that is often encountered in analog circuit design.

of the elementary circuits that is useful in many situations, just like the common-source amplifier with active load (Figure 10). Adding a cascode to a circuit is a powerful technique. For example, a common-gate combined with a common-source stage is depicted in Figure 11, and the cascade of two common-gate stages is illustrated in Figure 12. Of course, the essential common-gate stage qualifies as a two-transistor circuit as well (Figure 13).

The transmission gate (Figure 14) is an essential building block, allowing switching voltages and currents (a feat making the MOSFET such a valuable device). With a straightforward extension, a multiplexer can be constructed (Figure 15). However, in most practical implementations, a set of transmission gates will be applied for this purpose.

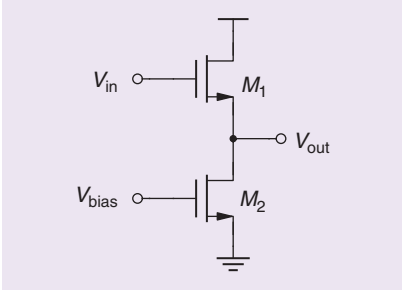

FIGURE 9: The source follower (or common-drain stage) utilizing M_2 as a current source to bias M_1.

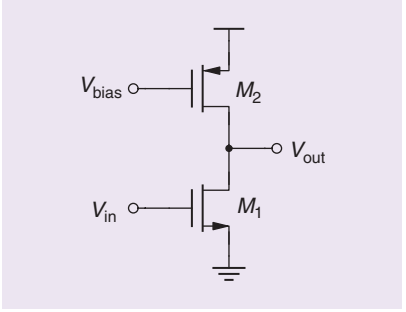

FIGURE 10: The common-source amplifier with active load.

Improved Basic Circuits

It has been realized that the digital inverter presented in Figure 1 can also be employed as an excellent low-voltage amplifier (V_{out}) or transconductance stage (I_{out}) when both transistors are biased in saturation. Shorting V_{in} and V_{out}, a replica bias is readily available [9].

Several low-voltage circuits can be implemented using the body terminal of a MOSFET as an additional

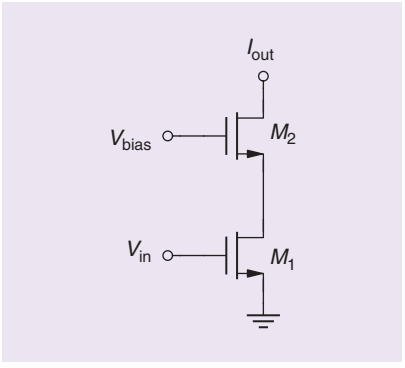

FIGURE 11: The cascoded common-source stage boosting the output impedance of M_1 considerably to $r_{out} \approx g_{m2}/(g_{ds1} \cdot g_{ds2})$.

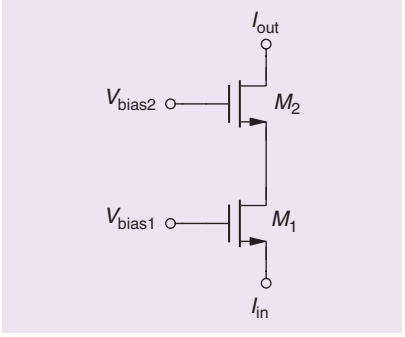

FIGURE 12: The cascoded common-gate stage. Note that $I_{out} \approx I_{in}$, but the impedance level changes drastically, creating gain or a high output impedance at the output node.

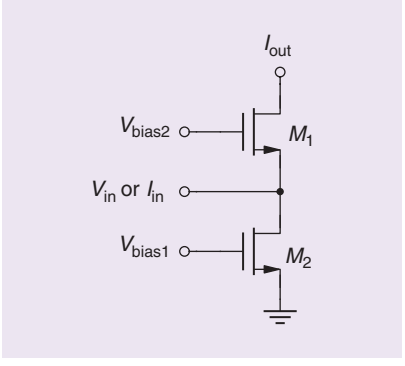

FIGURE 13: The common-gate stage employing M_2 as a current source to the bias transistor M_1.

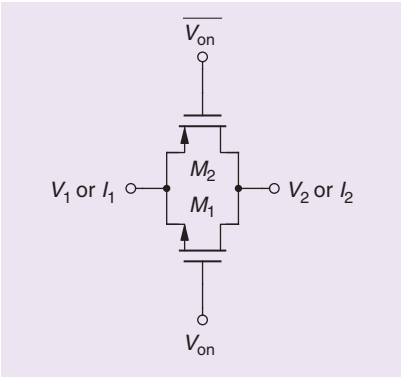

FIGURE 14: The transmission gate switches between V_1/I_1 and V_2/I_2 for both voltage and current (and it works rail to rail, too).

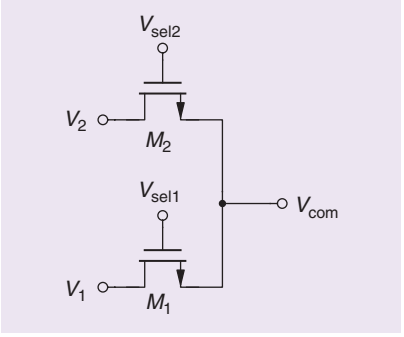

FIGURE 15: The two-to-one multiplexer connecting either V_1 or V_2 to V_{com}. Depending on V_{sel1} and V_{sel2}, the MOSFETs are alternately switched on or off.

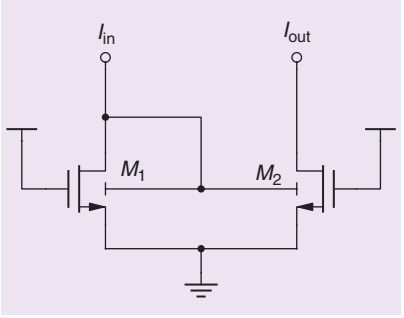

FIGURE 16: This circuit is an improved version of Figure 7 in that it allows a low-voltage operation of the current mirror, requiring a voltage headroom substantially less than V_{GS1} [12].

control input, like the low-voltage current mirror depicted in Figure 16. Some arrangements allow for precise voltage-gain and high-speed operation, as demonstrated by the circuits displayed in Figures 17 and 18.

Figure 19 presents an enhanced version of the source follower, also known as a *class-B* (*push/pull*) *amplifier*. Degeneration is a primary method to improve matching, noise figure, or output resistance. Different MOSFET-only implementations are feasible (Figures 20 and 21), with the implementation in Figure 21 allowing the performance to be tuned during operation by varying V_{bias}.

Combining a common-source stage with a common-gate topology [10], as illustrated in Figure 22, results in a differential-output transconductance stage with a single-ended low-ohmic input. It can thus be used under impedance-matched conditions, also providing some noise and linearity

Some arrangements allow for precise voltage-gain and high-speed operation.

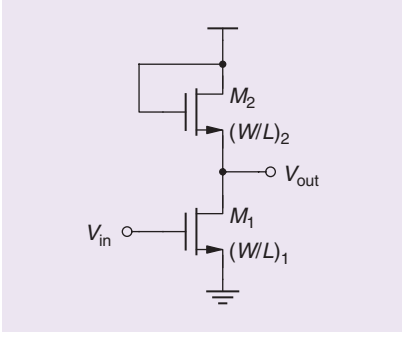

FIGURE 17: The common-source amplifier with diode load is sometimes called a *wide-band amplifier* due to its potentially high-speed operation. Here, the gain is set precisely at $A_v = V_{out}/V_{in} = -\sqrt{(W/L)_1/(W/L)_2}$, depending only on the transistor sizing (and neglecting the body effect).

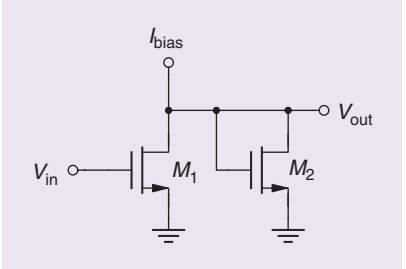

FIGURE 18: The folded version of Figure 17, which has the advantages of a removed body effect in M_2 and a ground-referred output node [13].

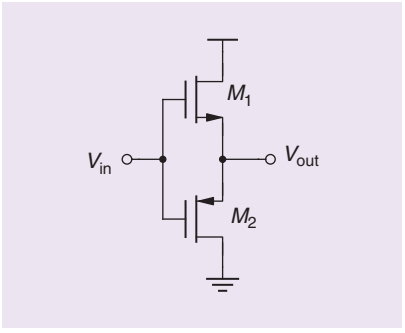

FIGURE 19: The class-B push-pull follower can be considered an enhanced version of the simple source follower presented in Figure 9. Lacking a class-A bias component, this structure is subjected to crossover distortion.

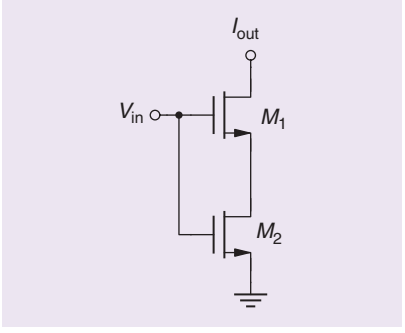

FIGURE 20: The MOSFET-R degenerated common-source stage. By appropriately sizing M_2, the degeneration can be adapted [13]. This arrangement using two transistors can also increase the length of a (compound) device (for example, in current mirrors) as, otherwise, a MOSFET with different L will not match well.

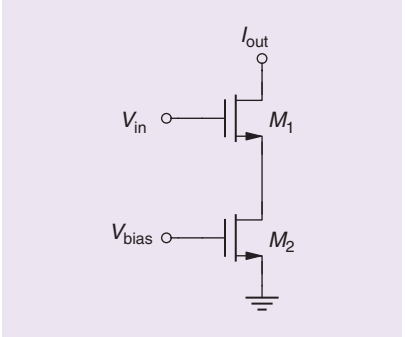

FIGURE 21: A variation of the implementation displayed in Figure 20, where the degeneration of M_1 can be adapted by tuning V_{bias}.

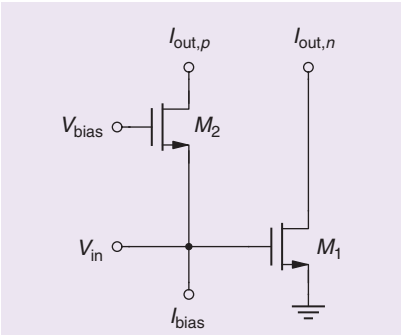

FIGURE 22: A common-gate, common-source topology offering impedance-matched, single-ended input and differential output while simultaneously canceling noise and distortion [11].

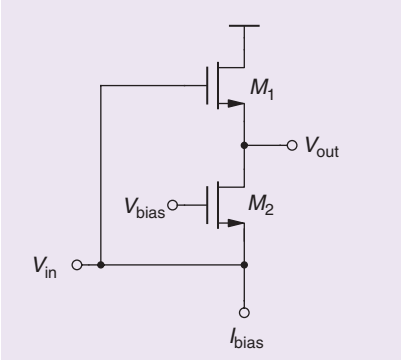

FIGURE 23: This low-noise amplifier was discovered by using an exhaustive search of potential two-transistor, wide-band amplifiers. For practical implementation, M_1 requires an ac coupling (and proper biasing) in its gate connection to keep M_2 in saturation [2].

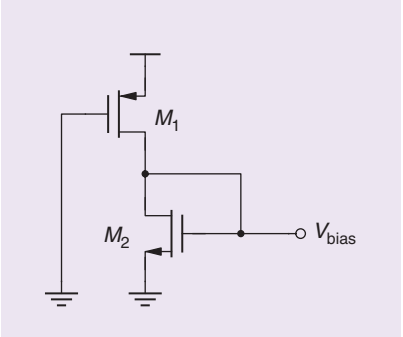

FIGURE 24: A (simple) bias-voltage generator using the current source M_1 to bias M_2 so that $V_{bias} = V_{GS2}$.

cancelation under the ideal bias [11]. In yet another twist, a source follower can be combined with a common-gate stage, resulting in a useful amplifier configuration (see Figure 23), which has been found by systematically generating graphs consisting of two transconductance stages [2].

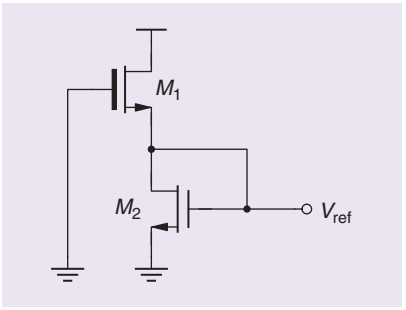

FIGURE 25: A constant bias-voltage generator (M_1 and M_2 must have different threshold voltages $V_{th1} \neq V_{th2}$) [14].

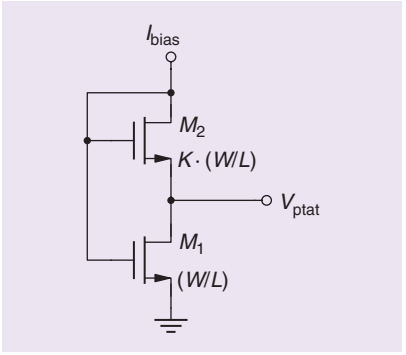

FIGURE 26: A proportional-to-absolute-temperature (PTAT) voltage generator if M_1 and M_2 are kept in subthreshold operation [15].

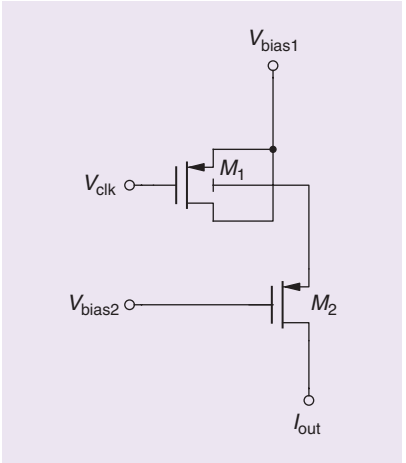

FIGURE 27: This pA current source is based on the periodic filling and flushing of Si–SiO_2 interface traps by alternating M_1 between accumulation and inversion (through the proper choice of V_{bias1} and V_{bias2} and the switching levels of V_{clk}). It can operate with reasonably high clock frequencies and still create tiny currents [16].

Biasing Circuits

The generation of a bias voltage is a task that is often encountered in analog circuit design. When the requirements on stability are moderate, a simple configuration, as displayed in Figure 24, might be sufficient. A surprisingly stable voltage reference can be constructed from two MOSFETs with different threshold voltages, as demonstrated in Figure 25. Occasionally, a bias voltage with a well-defined proportionality to temperature is needed, for example, in temperature-sensor circuits. This effect can be achieved by a PTAT voltage generator like the one depicted in Figure 26. Sometimes, circuits

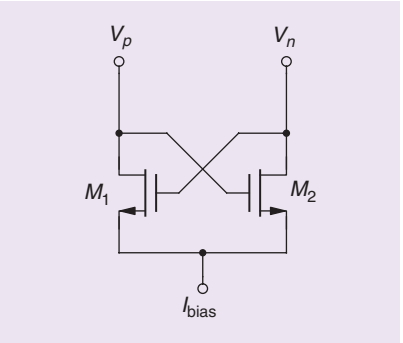

FIGURE 28: Two transistors with cross-coupling form a negative resistance between V_p and V_n and are mainly employed in oscillators and comparators. As in Figure 8, the bias-current source can be replaced by a fixed potential.

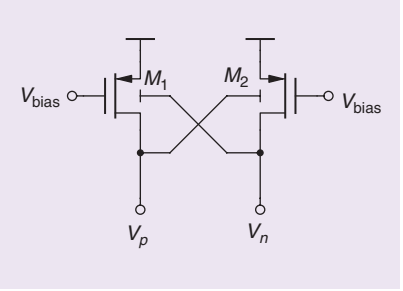

FIGURE 29: This circuit is a low-voltage version of Figure 28, where the body controls the MOSFET, avoiding the significant V_{GS} drop at V_p and V_n [18].

are based on obscure second-order effects, like charge trapping in the Si–SiO_2 interface traps, which are used in the clocked circuit displayed in Figure 27 and can create pA-currents in an area-efficient manner.

Diverse Circuit Elements

The various operating modes of a MOSFET can be utilized differently and lead to practical circuit elements. The cross-coupled differential pair (see Figures 28 and 29) synthesizes a negative resistance, which can cancel losses, for example, in oscillators

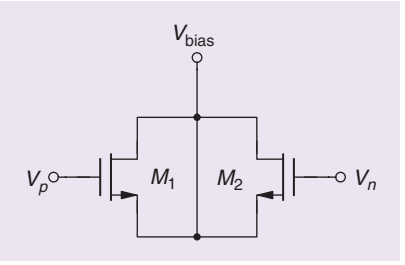

FIGURE 30: The varactor (the capacitance between V_p and V_n depends on the bias voltage V_{bias}) is often used in voltage-controlled oscillators. In most technologies, the NMOS can be put inside the n-well so that the varactor works in accumulation, providing an optimized tuning range and high Q [19].

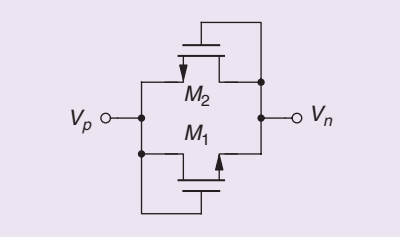

FIGURE 31: The antiparallel diodes can be employed for many things, for example, voltage clamping.

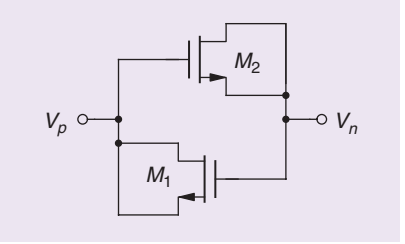

FIGURE 32: The antiparallel MOSFET capacitors make the differential capacitance more linear and symmetrical. As in Figure 30, an NMOS in n-well is an option.

or *Q*-enhanced *LC* filters. Since the effective capacitance between the gate terminal and the source/drain connection of a MOSFET is a function of biasing conditions, the arrangement demonstrated in Figure 30 can be employed as a varactor.

Using local feedback to create a MOSFET "diode," two antiparallel diodes can replace conventional *pn*-diodes, for example, in voltage limiters (Figure 31). The gate oxide of a MOSFET usually offers the highest capacitance density in a given CMOS technology, so an antiparallel pair of MOSFETs (see Figure 32) can substitute a linear capacitor with one that has mediocre linearity but is much smaller. This structure has the additional benefit of symmetrical parasitic capacitors at both terminals.

A surprisingly stable voltage reference can be constructed from two MOSFETs with different threshold voltages.

An active inductor can be simulated by transistors using gyrator principles [17], offering a significant area reduction compared to what's offered by a passive implementation based on a coil constructed from the metal layers. An exemplary implementation based on two MOSFETs is displayed in Figure 33.

Analog Signal Processing

The processing of analog signals is often needed when devising circuits. The area-efficient division of voltages (see Figure 34) or currents [either employing a current mirror (as in Figure 7) or the advanced usage of the Bult current divider (presented in Figure 35)] can become handy. In most implementations of an analog-to-digital converter, a sample-hold stage is required, which often exploits the excellent switching capabilities of the MOSFET, as demonstrated in Figure 36, where a MOSFET configured as a capacitor stores the sampled voltage. Sampling can be used for frequency conversion, which can also be achieved through the arrangement in Figure 37, where the time-variant

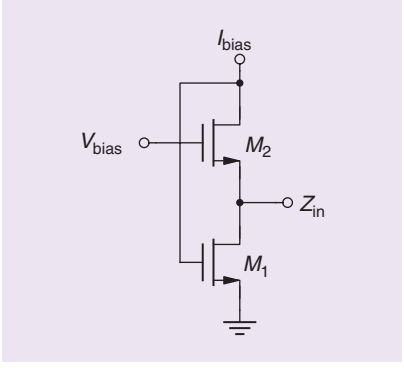

FIGURE 33: This circuit, which is a similar configuration of the flipped voltage follower in Figure 47, can function as an active inductor, providing $L = C_{GS1}/(g_{m1} \cdot g_{m2})$ [20].

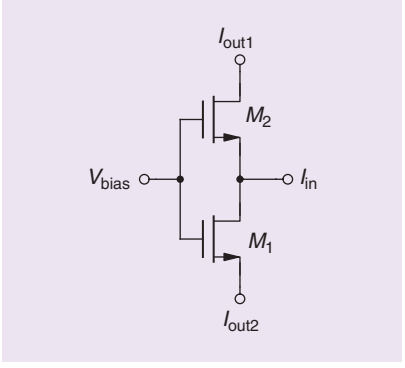

FIGURE 35: The Bult current divider (if M_1 and M_2 are of identical size, then I_{in} is precisely split in half between I_{out1} and I_{out2}) [22].

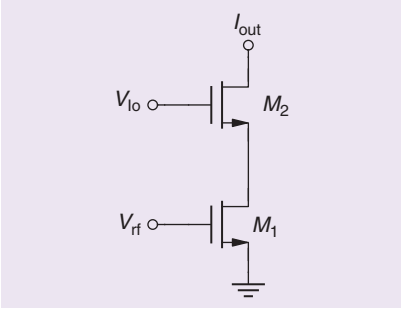

FIGURE 37: In the dual-gate MOSFET (a similar arrangement as in Figure 11), the periodic local-oscillator signal V_{lo} causes the time-variant change of the transconductance of M_1, resulting in a frequency conversion from the input V_{rf} to the output I_{out} [21].

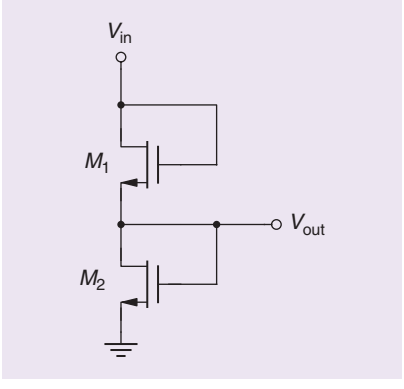

FIGURE 34: An area-efficient voltage divider. If M_1 and M_2 are the same size, then $V_{out} \approx V_{in}/2$. Often, a PMOS version is a better choice since it can avoid the body effect by tying the body to the respective source for M_1 and M_2.

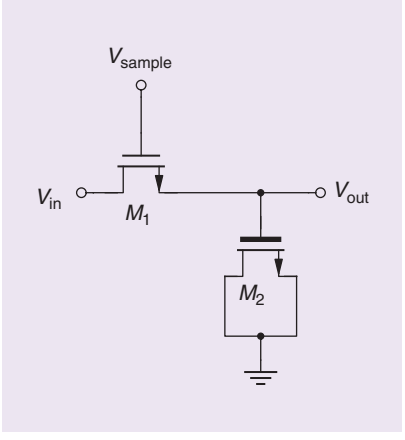

FIGURE 36: A sample-and-hold circuit implementing the gate capacitance of M_2 as a storage capacitor (a low to zero V_{th} would be an advantage in this case) [23].

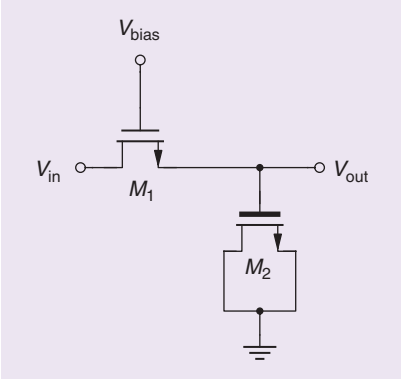

FIGURE 38: The circuit of Figure 36 becomes a continuous-time, low-pass filter if M_1 gets a fixed bias instead of a clock signal. Note that this circuit transforms into a high-pass filter when M_1 and M_2 are swapped.

Circuits working with the body terminal as a fourth control input can add many possibilities.

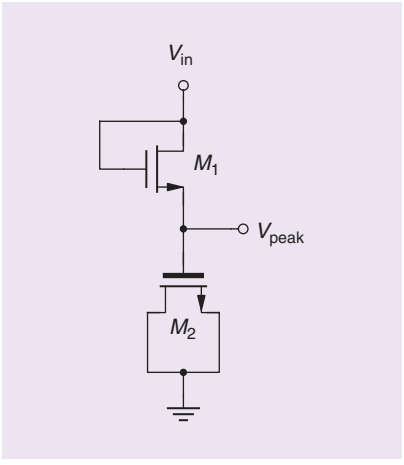

FIGURE 39: A voltage-peak detector, where $V_{peak} = V_{in,max} - V_{gs1}$.

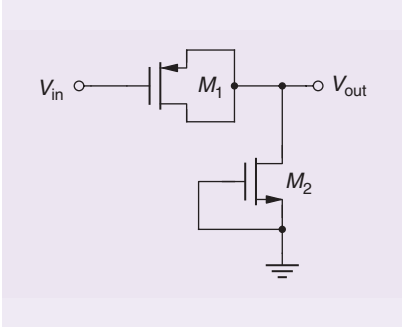

FIGURE 40: A similar circuit to Figure 39, which can function as an approximate voltage doubler when driven by a sinusoidal input voltage. On negative swings of V_{in}, the capacitor M_1 gets charged to $|V_{in}| - V_{gs2}$, which is added to V_{in} during positive swings when M_2 is off. As with any circuit with negative voltages, proper connection of the wells is required [24].

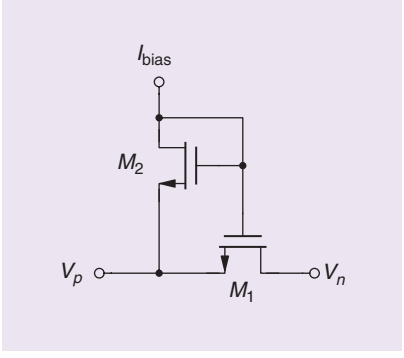

FIGURE 41: The controlled (high-impedance) floating resistor.

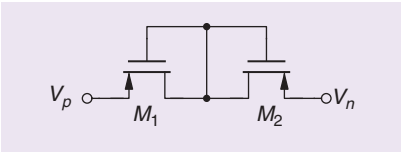

FIGURE 42: This arrangement creates an enormous resistance between V_p and V_n, although it is also susceptible to temperature and process variations [25].

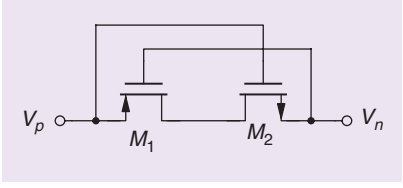

FIGURE 43: The ultralow-power diode (ULPD) with reduced leakage in the reverse direction [26].

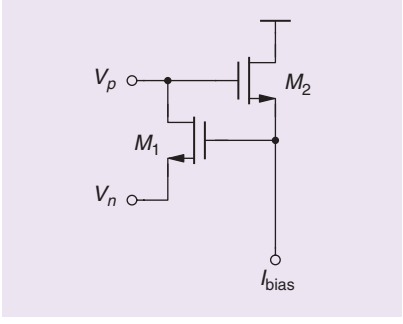

FIGURE 44: The floating level shift (or "floating battery") effectively shifts a bias point between V_p and V_n as $V_{shift} = V_p - V_n = V_{GS1} + V_{GS2}$.

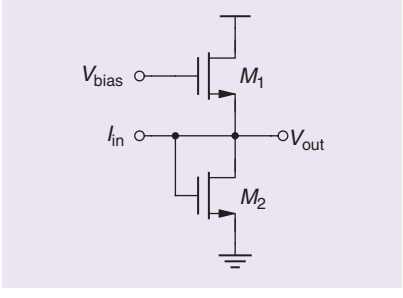

FIGURE 45: This circuit is a perfectly linear I-to-V converter with $V_{out}/I_{in} = [\mu C_{ox} \cdot (W/L) \cdot (V_{bias} - 2V_{th})]^{-1}$ if we assume a square-law behavior, and M_1 and M_2 are the same size and kept in saturation (and neglecting body effect) [27].

change of the transconductance of M_1 causes a mixing effect [21].

Realizing the MOSFET operating as a controlled resistor in the triode region, Figure 36 can be easily transformed into a (programmable) low-pass filter, as illustrated in Figure 38. By rewiring the sampling switch into the diode-equivalent MOSFET configuration, a voltage-peak detector (Figure 39) and an approximate voltage doubler (Figure 40) can be built for ac signals.

Simple Circuits With a Twist

While most CMOS processes provide thin-film resistors, it is often difficult to realize values in the MΩ to GΩ range. The MOSFET in triode or off-state (Figures 41 and 42) is a good alternative at a much smaller silicon area. An improved version of a diode-connected MOSFET is demonstrated in Figure 43. This two-transistor construction, called the

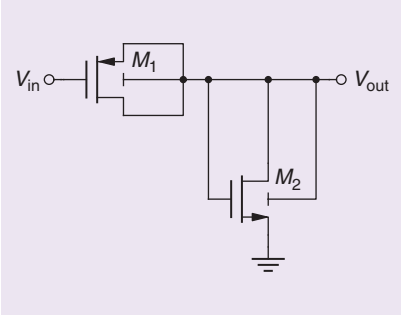

FIGURE 46: This circuit shifts a digital input voltage V_{in} to an output voltage V_{out} swinging around V_{SS} [28].

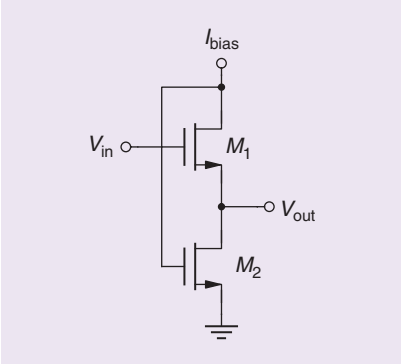

FIGURE 47: The flipped voltage follower is an improved version of Figure 9, employing feedback to lower the output impedance to $r_{out} = g_{ds2}/(g_{m1} \cdot g_{m2})$ [29].

ULPD, considerably lowers the leakage current in the reverse direction. A level shift is often needed in a signal path, which can be implemented as pictured in Figure 44. Sometimes a simple circuit shows a surprising property, and the linear *I*-to-*V* converter illustrated in Figure 45 is such an example.

Compensating for the low β of the parasitic BJT can be achieved by implementing the structure depicted in Figure 50.

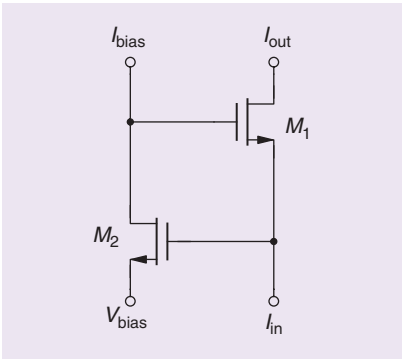

FIGURE 48: The regulated cascode increasing the effect of the cascode M_1 by g_{m2}/g_{ds2} due to feedback. Note that the source of M_2 can be tied to the ground if combined with a common-source input stage [30].

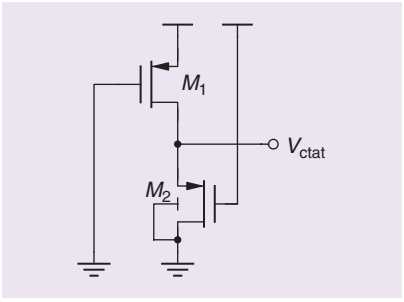

FIGURE 49: This simple CTAT voltage generator can be created by exploiting the parasitic (lateral or vertical) PNP transistor inherent in a PMOS structure [31].

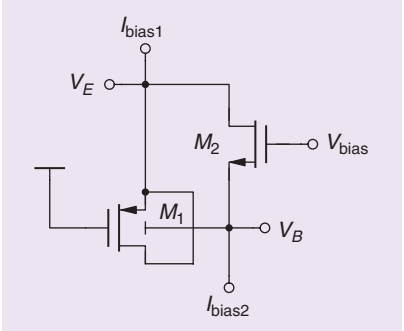

FIGURE 50: The parasitic BJT introduced in Figure 49 often suffers from poor β. This circuit forces the collector current of the parasitic (vertical) p-n-p to $I_C = I_{bias1} - I_{bias2}$, although the collector terminal (being the p-substrate) is not accessible. By doing this, the resulting $V_{EB} = V_E - V_B$ can be accurately employed in a bandgap circuit [32].

Using the MOSFET as a BJT

Inherent to the physical structure of a MOSFET is a bipolar junction transistor (BJT), which often shows inadequate performance, like poor current gain $\beta \ll 10$. Still, it can be employed to generate a temperature-dependent voltage, like the circuit presented in Figure 49, whose proportional-to-complementary-temperature (CTAT) property is an excellent addition to the PTAT behavior of the circuit in Figure 26. Compensating for the low β of the parasitic BJT can be achieved by implementing the structure depicted in Figure 50, which improves the accuracy of a bandgap circuit built from these augmented BJT devices.

Conclusions

Fifty practical circuit snippets employing just two MOS transistors have been presented. The motivation behind this compilation is to celebrate the creativity in analog circuit design and to demonstrate the versatility of the fabulous MOSFET. Walking through these examples (and considering that this compendium is far from complete [3]) leaves one in awe as one thinks about the endless possibilities that are generated when an analog circuit designer is given a handful of these fantastic transistors.

Acknowledgments

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