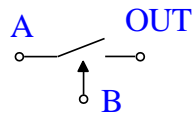## Transmission gate and Pass-Transistor Logic

► Advanced logic function or switching scheme are implemented using the feature of transistor MOS to work as a simple switch

► It has the advantage of being simple and fast. Complex gates are implemented with the minimum number of transistors (the reduced parasitic capacitance results in fast circuits

A   OUT

B

$$OUT = A \cdot B$$

► The static and transient performance strongly depend upon the availability of an high quality switch with low parasitic resistance and capacitance
   * A single transistor is used as switch: *Pass Transistor*
   * N- and P-transistor are used: *Transmission Gate*

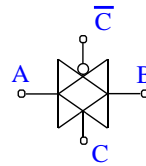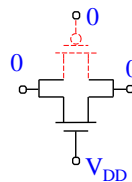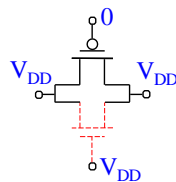► Implementation with a single transistor reduces the noise margin and causes static power consumption

V_{DD} $V_{DD}-V_{tn}$ 0 $-V_{tp}$ V_{DD} $V_{DD}-V_{tn}$ V_{DD} OUT

V_{DD} 0 V_{DD}

1
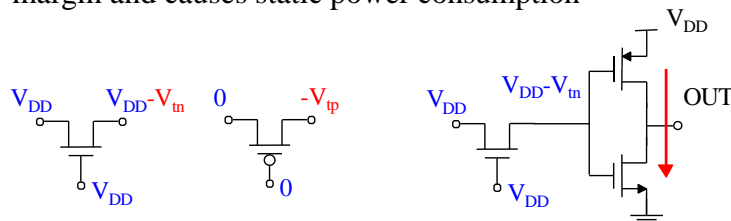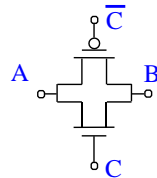
Transmission Gate

Transmission Gate Simbol

$\overline{C}$

A — B

C

$\overline{C}$

A — B

C

▶ Transmission gate has better noise margin than pass transistor

0

V_{DD} — V_{DD}

V_{DD}

0

0 — 0

V_{DD}

▶ Transmission gate is very efficient to implement some complex gate (MUX, DEMUX and XOR)

2-input Multiplexer
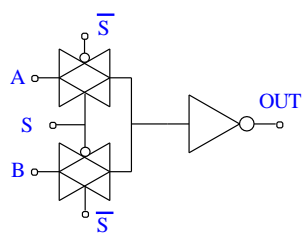
4-input Multiplexer

$\overline{S}$

A

S

B

$\overline{S}$

OUT

$$\overline{OUT} = A \cdot S + B \cdot \overline{S}$$

$\overline{X}$　$\overline{Y}$

A

X　　Y

B

$\overline{X}$　$\overline{Y}$

C

X　　Y

D

$\overline{X}$　$\overline{Y}$

OUT

$$\overline{OUT} = A \cdot X \cdot Y + B \cdot \overline{X} \cdot Y + C \cdot X \cdot \overline{Y} + D \cdot \overline{X} \cdot \overline{Y}$$

2
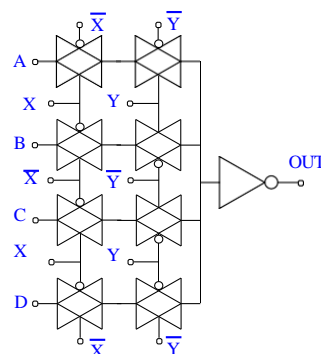
4-input MUX as cascade of 2-input MUX
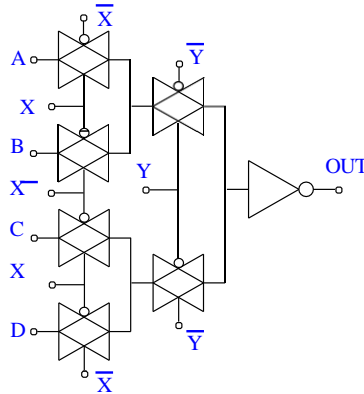
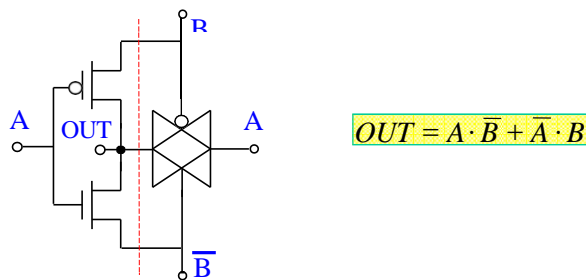$$\overline{OUT} = A \cdot X \cdot Y + B \cdot \overline{X} \cdot Y + C \cdot X \cdot \overline{Y} + D \cdot \overline{X} \cdot \overline{Y}$$

► More parasitic capacitances on internal nodes, less on the output node

2-input XOR

► Can be implemented with a 2-input MUX, or:
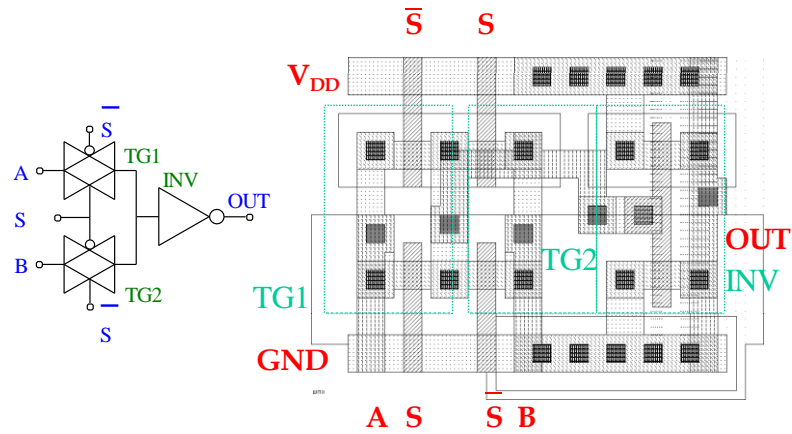

$$OUT = A \cdot \overline{B} + \overline{A} \cdot B$$

► Only the left side can implement the XOR logic function, but a threshold voltages is lost at the output without implementing the right side circuit

Transmission Gate MUX Layout
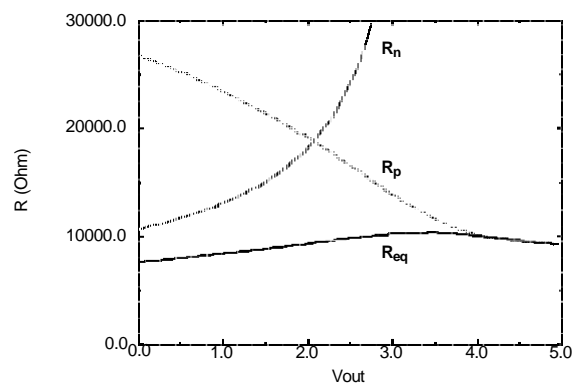
$\overline{S}$ S

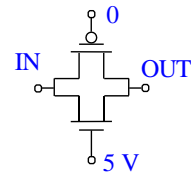V_{DD}

TG1

INV

A

S

B

TG2

S

OUT

TG2

TG1

OUT

INV

GND

A S $\overline{S}$ B

Transmission Gate Resistance

R_n

R_p

R_{eq}

R (Ohm)

30000.0

20000.0

10000.0

0.0

0.0   1.0   2.0   3.0   4.0   5.0

Vout

$(W/L)_p = (W/L)_n =$

1.8/1.2

0

IN   OUT

5 V

4

► Despite the nonlinear behavior of the NMOS and PMOS transistors varying the input voltage, *the resistance of a transmission gate is almost constant*

► We can approximate its value with that given by the parallel of transistor resistances, assuming both in linear region

$$\frac{1}{R_{eq}} = G_{eq} = \left.\frac{dI_D}{dV_{DS}}\right|_n + \left.\frac{dI_D}{dV_{DS}}\right|_p =$$

$$= \beta_n(V_{GSn} - V_{tn} - V_{DSn}) + \beta_p\left(V_{SGp} + V_{tp} - V_{SDp}\right)$$

► If the gate-source voltage is around $V_{DD}/2$, the two transistors are in linear region ($V_{DS} \approx 0$)

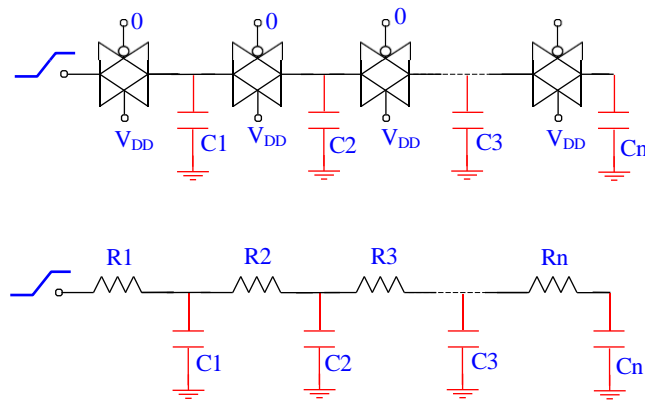$$\frac{1}{R_{eq}} = \beta_n\left(\frac{V_{DD}}{2} - V_{tn}\right) + \beta_p\left(\frac{V_{DD}}{2} + V_{tp}\right)$$

► Assuming the threshold voltage and the gain factor of the NMOS and PMOS are equal (PMOS twice the NMOS)

$$R_{eq} = \frac{1}{nC_{ox}(W/L)_n(V_{DD} - 2V_t)}$$

► To reduce parasitic effects both transistors are generally minimum size

Transmission Gate Delay

► Applying the *open-circuit time constant*

$$\tau = \sum_{i=1}^{n} C_i \sum_{j=1}^{i} R_j = RC \sum_{i=1}^{n} i = RC \frac{n(n+1)}{2}$$
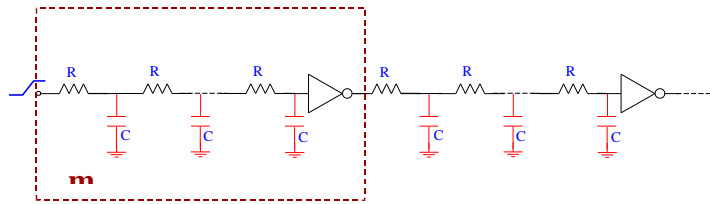
$R=R_{eq}$ and $C=4(C_{gs}+C_{sb})$

► Approximating the circuit with a pole-dominant behavior $\tau_{PD} = 0.69\,\tau$. *It increase with the square of n*

► We can introduce buffer to minimize τ_{PD}

$$\tau_{PD} = 0.69\left[\frac{n}{m}RC\frac{m(m+1)}{2}\right] + \left(\frac{n}{m}-1\right)\tau_{PDinv}$$

$$\frac{d}{dm}\tau_{PD} = 0$$

$$0.69RC\frac{n}{2} - \frac{n}{m^2}\cdot\tau_{PDinv} = 0$$

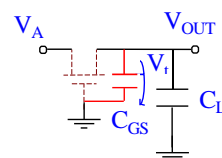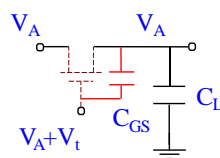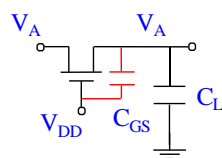$$m_{opt} = \sqrt{\frac{2\tau_{PDinv}}{0.69RC}}$$

Typical value 3-4

Source of errors

► *Clock feedthrough* due to capacitive coupling

Transistor ON　　　　　　Transistor OFF

Charge conservation yields
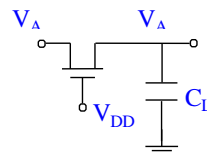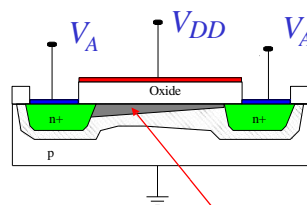
$$(C_L + C_{GS})V_{OUT} = C_L V_A - C_{GS}V_t$$

$$\Delta V_{OUT1} = V_{OUT} - V_A = -\frac{C_{GS}}{C_L + C_{GS}}(V_{A+V_t})$$

Reduce with the reduction of C_{GS}

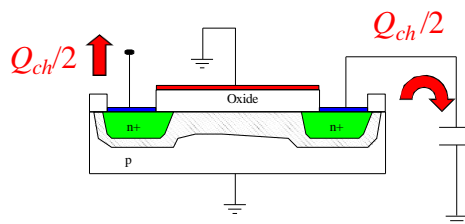► *Charge Injection* due to redistribution of the charge in the channel

Transistor ON (triode region)

$$Q_{ch} = C_{ox}WL(V_{DD} - V_A - V_t)$$

When the transistor switch off the charge in the channel is lost. If the clock edge are sufficiently steep the charge distribute equally on the two diffusion node

$Q_{ch}/2$ $Q_{ch}/2$

$$\Delta V_{OUT2} = -\frac{1}{2}\frac{C_{ox}WL(V_{DD}-V_A-V_t)}{C_L}$$

► *Clock feedthrough* and *Charge Injection* are lower reducing the transistor dimensions (i.e., W and L)

► Both the errors are reduced in Transfer Gates if the transistor are of equal dimensions.

     * the charge in the channel of equal NMOS and PMOS transistors are equal but with opposite sign

     * If NMOS and PMOS transistors are equal and switch off symmetrically the charge in the C_{GS} are equal but opposite

NMOS-Only TG with Level Restorer

► Noise margin reduction of a pass transistor is avoided with a PMOS transistor in positive feedback which restores the output value from V_{DD}- V_t to V_{DD}
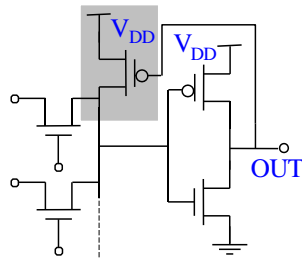
► Only a PMOS transistor is needed for a set of TG which have a common output node

► *Clock feedthrough* and *Charge Injection* are higher than than in complementary TG

► Reduce the static power consumption of the next inverter but introduce a contribute due to itself

► Design strategy is close to that of ratioed logic

Design of an NMOS-Only TG

► The critical case is when the inner node was previously restored to V_{DD} (output voltage equal to 0), the first inverter has the input to V_{DD} and MR goes from 0 to V_{DD}

► During the transient a direct path between the power supply and ground exists

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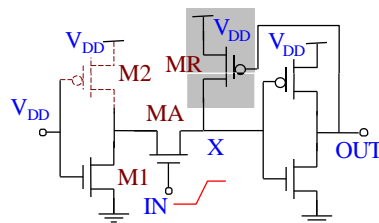
► To change the output state node X must be lower than the inverter threshold voltage $V_{DD}/2$ (the positive feedback complete the inverter commutation)

► To guarantee the above condition consider the Pseudo NMOS gate M1-MA-MR
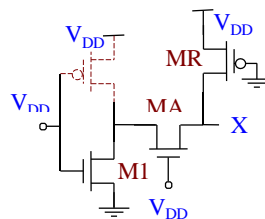
Transistor PMOS is in triode region

$$\frac{\frac{W_n}{L_{M1}+L_{MA}}}{(W/L)_{MR}} = \frac{[2(V_{DD}+V_{tp})-(V_{DD}-V_{OL})](V_{DD}-V_{OL})}{[2(V_{DD}-V_{tn})-V_{OL}]V_{OL}}\frac{\mu_p}{n}$$

$$\frac{\frac{W_n}{L_{M1}+L_{MA}}}{(W/L)_{MR}} = \frac{\mu_p}{\mu_n}$$
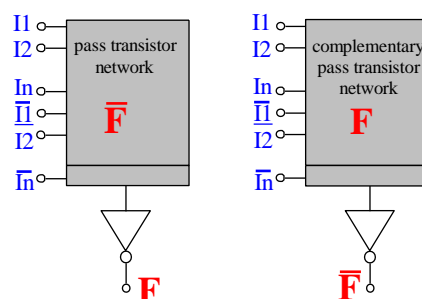
▶ If M1-MA are minimum size transistors

$$\boxed{\left(\frac{W}{L}\right)_{MR} \leq \frac{W_{min}}{L_{min}}}$$

CPL
(Complementary Pass-Transistor Logic)

▶ The logic is differential since two complementary data path are implemented

► Although differential signal requires extra circuitry, the differential style results advantageous in term of transistor number to implement some complex gates such as adders

► The availability of both polarity of every signal eliminates the need for extra inverter (addition speed up).

► The design is very modular. All gates use exactly the same topology, only the input are permutated. Complex gates are implemented with cascade of standard modules
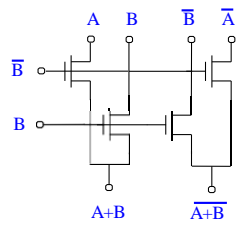
► NMOS transistors with $V_{tn}<-V_{tp}$ are needed to avoid static power consumption. (The reduced threshold improve the switching speed)
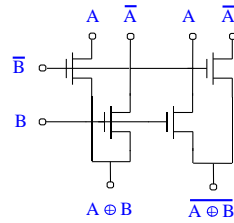
► The low V_{tn} leads higher subthreshold current

higher power supply

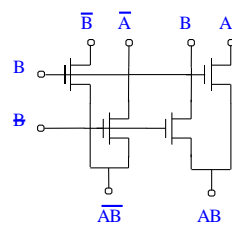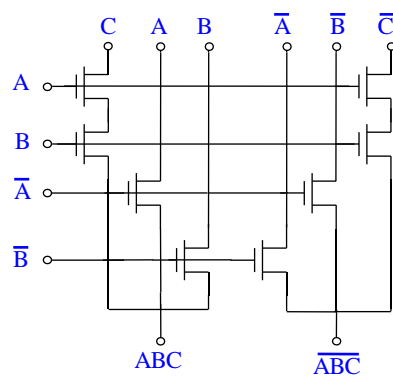► The low V_{tn} determines higher noise margin

2-input OR/NOR

A   B $\overline{B}$ $\overline{A}$

$\overline{B}$

B

A+B $\overline{A+B}$

2-input XOR/XNOR

A $\overline{A}$ A $\overline{A}$

$\overline{B}$

B

A $\oplus$ B $\overline{A \oplus B}$

2-input AND/NAND

$\overline{B}$ $\overline{A}$ B   A

B

B

$\overline{AB}$ AB

3-input AND/NAND

C   A   B $\overline{A}$ $\overline{B}$ $\overline{C}$

A

B

$\overline{A}$

$\overline{B}$

ABC $\overline{ABC}$

3-input OR/NOR

C   A   B $\overline{A}$ $\overline{B}$ $\overline{C}$

$\overline{A}$

$\overline{B}$

A

B

A+B+C $\overline{A+B+C}$

14
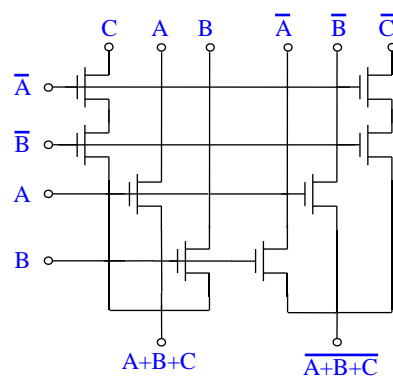
Layout of a 4-input NAND CPL

15