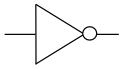
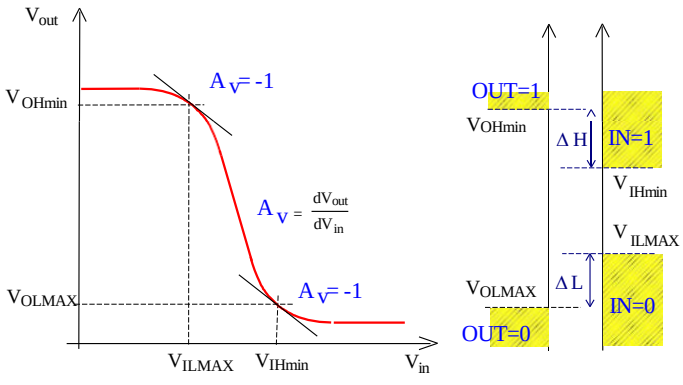
Inverter static characteristic



- *Voltage transfer characteristic V_{out}/ V_{in}*
- *Input characteristic I_{in} = f(V_{in})*
- *Output characteristic I_{out} = f(V_{out})*
- *Input Logic swing*
- *Output logic swing*
- *Logic threshold*
- *Noise margins*

Transfer characteristic and logic swing

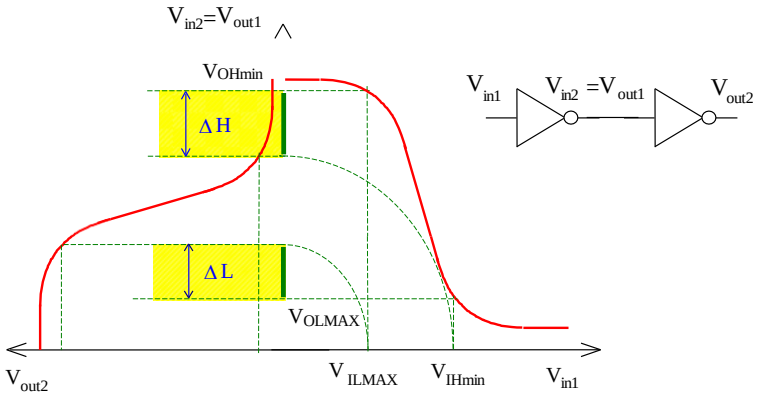


- *Input logic swing V_{IHmin} - V_{ILMAX}*
- *Output logic swing V_{OHmin} - V_{OLMAX}*

➡ The *Logic swing* is the lowest

Noise margin

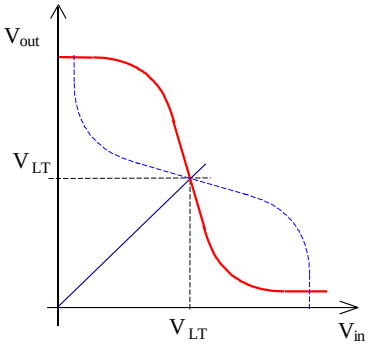
- represent the levels of noise that can be sustained when gates are cascaded (noise in the digital domain means unwanted variations of voltages and currents at the logic nodes)

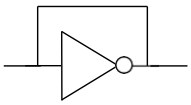


- *Noise margin low*: $\Delta L = V_{ILMAX} - V_{OLMAX} \approx V_{ILMAX} - V_{OL}$
- *Noise margin high*: $\Delta H = V_{OHmin} - V_{IHmin} \approx V_{OH} - V_{IHmin}$
- Must be: $V_{OHmin} > V_{IHmin} > V_{ILMAX} > V_{OLMAX}$
- ΔL and ΔH are a percentage of the logic swing and increase increasing the output logic swing
- For equal logic swing, ΔL and ΔH are higher in gate with small signal gain higher (in module)
- ΔL and ΔH are higher in gate with symmetric transfer characteristic

Logic threshold

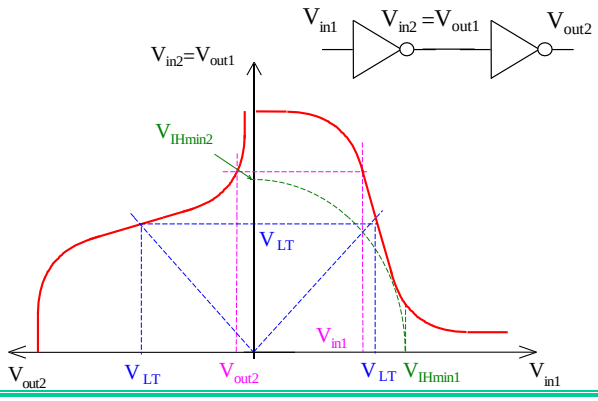
- Is the input value which gives the output of the same value $V_{in} = V_{out}$
- can be obtained with the output of the gate short-circuited with the input





Regenerative property

- a disturbed signal gradually converges back to one of the nominal voltage level after passing through a number of logical gates



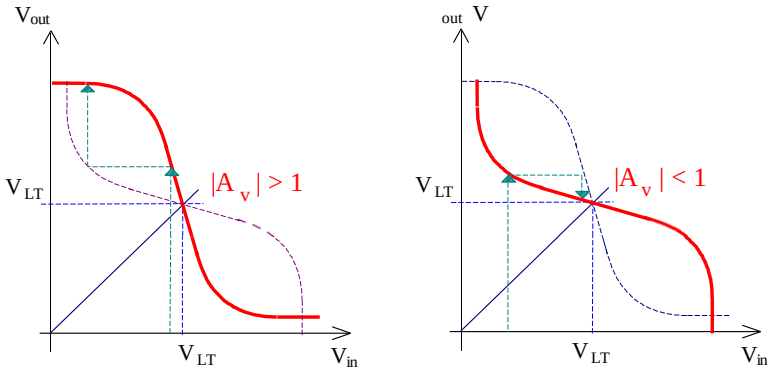
$V_{in1} = V_{LT} - \delta_1$

$V_{in2} = V_{out1} = V_{LT} + \delta_2$

$V_{out2} = V_{LT} - \delta_3$

$\delta_1 < \delta_2 < \delta_3$

- To have the *regenerative property* the module of the gain A_v around the logic threshold must be higher than 1



Fan-In and Fan-Out

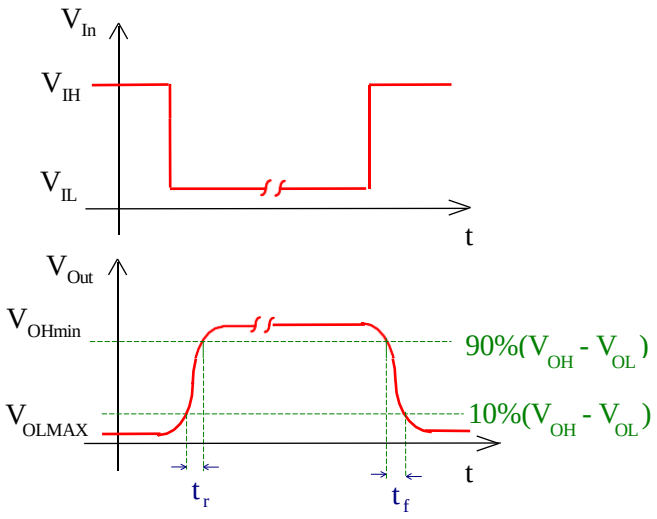
- ***Fan-Out***: number of load gates that are connected to the output
- Increasing the *Fan-Out* can affect the logic output level of the gate and/or, like in CMOS gates, can affect the dynamic performance of the driving gate

- ***Fan-In***: number of inputs to the gate

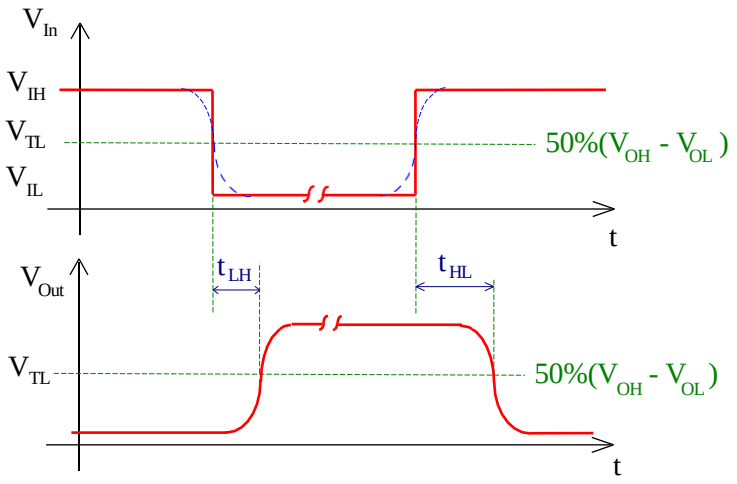
Inverter dynamic characteristic

- *Rise time*
- *Fall time*
- *Low-to-High (rise) delay*
- *High-to-Low (fall) delay*
- *Propagation delay (delay time)*

Rise and Fall time



Rise and Fall Delay



Propagation delay

$$t_{PD} = \frac{t_{LH} + t_{HL}}{2}$$

- It is used to define how quickly a gate responds to an input change
- In a symmetric gate (where $t_{LH} = t_{HL}$) $\boldsymbol{t_{PD}} = t_{LH} = t_{HL}$
- In CMOS $t_f \approx 2\ t_{HL}$ and $t_r \approx 2\ t_{LH}$, ⇒ $t_{PD} = \frac{t_f + t_r}{4}$

Power dissipation

Determines

- the heat dissipated by the circuit
- the energy consumed per operation

Influences

- Packaging
- cooling requirements
- supply-line sizing
- power-supply capacity
- the number of circuits that can be integrated onto a single chip

Hence, it affects

- feasibility
- cost
- reliability

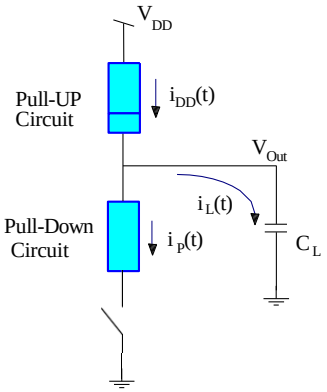
Peak Power : $P_{peak} = i_{peak} V_{supply} = \max(P)$

- set the supply-line size

Average Power : $P_{av} = \frac{1}{T}\int_0^T P(t)dt = \frac{V_{supply}}{T}\int_0^T i_{supply}(t)dt$

- predominantely affects cooling or battery requirements

Dynamic consumption



- During a low-to-high transition the energy given by the power supply is

$$E = \int_0^{\infty} V_{DD} i_L(t) dt = V_{DD} C_L \int_{V_{OL}}^{V_{OH}} dV = C_L V_{DD} (V_{OH} - V_{OL})$$

- Half is stored in the load capacitor and half is lost in the pull-up circuit
- During the high-to-low transition capacitor loss its charge and the associated energy

- each switching cycle (L→H→L) takes the energy

$$C_L V_{DD} (V_{OH} - V_{OL})$$

- if $V_{OH} = V_{DD}$ and $V_{OL} = 0$ during a switching cycle T the dynamic power is

$$P_d = \frac{E_d}{T} = C_L V_{DD}^2 f$$

The dynamic power

- depend only on the load capacitor, the power supply and the frequency
- increase with the square of the power supply

Static consumption

- May exists when the circuit is not switching

$$P_{st} = V_{DD} \frac{i_p(t_H)T_H + i_p(t_L)T_L}{T_H + T_L}$$

- if exist is the dominant source of power dissipation

Second order static consumption are due to

- current leakage of reverse-biased diodes
- subthreshold current in CMOS tecnologies

Power-Delay product

- There is a trade-off between the delay (i.e., speed) and the power consumption of a gate
- the *power-delay product* has been introduced to evaluate the efficiency of the gate
- it is simply the energy consumed by the gate for switching event
- if the dynamic consumption is the dominant term of dissipation the power delay is $C_L V_{DD}^2$