

Inverter Voltage Transfer Characteristic

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Introduction

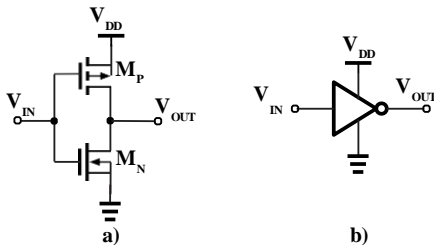


Figure 1: a) Schematic of a CMOS inverter; b) Symbol for the CMOS inverter

- The CMOS Inverter is the nucleus of the digital design
- More complex gates design can be reduced to an equivalent inverter
- The static behaviour is found in the Voltage Transfer Characteristic (VTC) curve, in which is reported V_{OUT} vs. V_{IN}

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Voltage Transfer Characteristic (VTC)

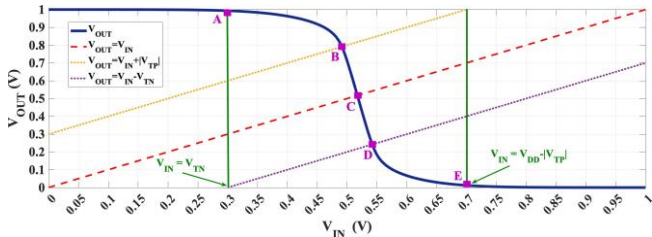


Figure 2: VTC curve for a CMOS inverter with 50nm minimum length technology

- $V_{DD} = 1.0\text{V}$, $V_{TN} \approx |V_{TP}| = 0.3\text{V}$
- $V_{IN} \in [0 - 1.0]\text{V}$
- $(W/L)_N = 100/50\text{ (nm/nm)}$
- $(W/L)_P = 200/50\text{ (nm/nm)}$

Voltage Transfer Characteristic (VTC)

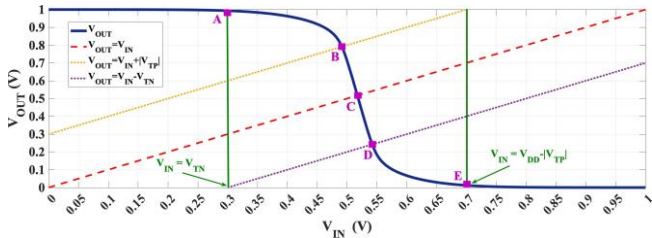


Figure 3: VTC curve for a CMOS inverter with 50nm minimum length technology

Green vertical strict lines

- If $V_{IN} < V_{TN}$, M_N is OFF since $V_{GS} < V_{TN}$
- If $V_{IN} < V_{DD} - |V_{TP}|$, M_P is OFF since $V_{SG} < |V_{TP}|$

Voltage Transfer Characteristic (VTC)

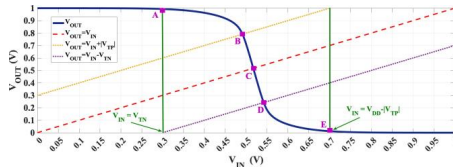


Figure 4: VTC curve

Yellow and Purple strict lines

- If $V_{DG} < |V_{TP}|$, M_P is in saturation region (area below the yellow line, until $V_{IN} = V_{DD} - |V_{TP}|$) (from point B to point E)
- If $V_{GD} < |V_{TN}|$, M_N is in saturation region (area above the purple line, until $V_{IN} = V_{TN}$) (from point A to point D)
- $V_D = V_{OUT} = y$ and $V_G = V_{IN} = x$ for both NMOS and PMOS transistor
- EX: $V_{DG} = V_D - V_G = V_{OUT} - V_{IN}$. PMOS in saturation
 $\rightarrow V_{DG} < |V_{TP}| \rightarrow V_{OUT} - V_{IN} < |V_{TP}| \rightarrow y < x + |V_{TP}|$ (area below the yellow line)

VTC : Point A

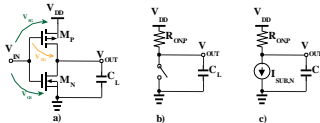


Figure 5: a) CMOS Inverter; b) Equivalent model 1; c) More detailed equivalent model 1

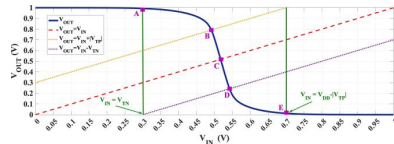


Figure 6: VTC CMOS inverter

- $V_{IN} < V_{TN}$: M_N is OFF (open switch) and M_P is ON
- $V_{DG,P} > |V_{TP}|$ (area above the yellow line) $\rightarrow M_P$ is in triode region, equivalent to $R_{ON,P}$
- The output capacitor, C_L , is charged through $R_{ON,P}$
- While V_{IN} increases, the sub-threshold leakage current of M_N ($I_{SUB,N}$) starts discharging C_L

VTC : From Point A to Point B

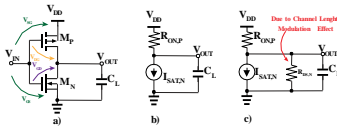


Figure 7: a) CMOS Inverter; b) Equivalent model 2; c) More detailed equivalent model 2

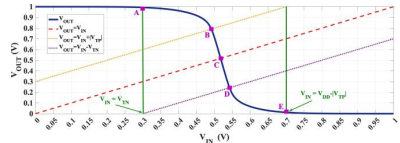


Figure 8: VTC CMOS inverter

- $V_{IN} > V_{TN}$: M_N is ON (point A) and M_P is ON
- $V_{DG,P} > |V_{TP}|$ (area above the yellow line) $\rightarrow M_P$ is in triode region, equivalent to $R_{ON,P}$
- The output capacitor, C_L , is charged through $R_{ON,P}$
- C_L is discharged by M_N ($I_{SAT,N}$) since it works in saturation region ($V_{GD} < V_{TN}$, area above the purple line)
- Point B : M_P enters the saturation region $V_{DG} = |V_{TP}|$

VTC : From Point B to Point D

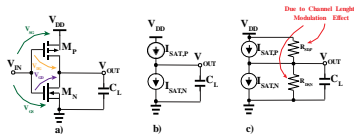


Figure 9: a) CMOS Inverter; b) Equivalent model 3; c) More detailed equivalent model 3

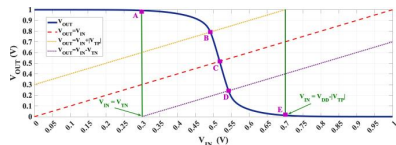


Figure 10: VTC CMOS inverter

- Both Transistors are ON but in saturation region
- $V_{DG,P} < |V_{TP}|$ (area below the yellow line)
- $V_{GD,N} < V_{TN}$ (area above the purple line);
- Point C : $V_{OUT} = V_{IN} = V_{TL}$, V_{TL} is the threshold logic value (about $V_{DD}/2$)

VTC : From Point D to Point E

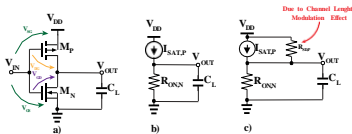


Figure 11: a) CMOS Inverter; b) Equivalent model 4; c) More detailed equivalent model 4

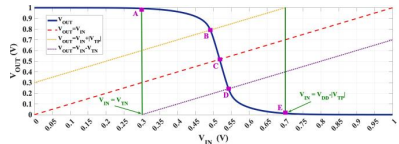


Figure 12: VTC CMOS inverter

- $V_{IN} < V_{DD} - |V_{TP}|$, M_P is ON and M_N is ON
- $V_{GD,N} > V_{TN}$ (area below the purple line) $\rightarrow M_N$ is in triode region, equivalent to $R_{ON,N}$
- The output capacitor, C_L , is discharged through $R_{ON,N}$
- C_L is charged by M_P ($I_{SAT,P}$) since it works in saturation region ($V_{DG} < |V_{TP}|$, area below the yellow line)
- Point E: M_P enters the cut-off region $V_{SG} = |V_{TP}|$

VTC : Point E

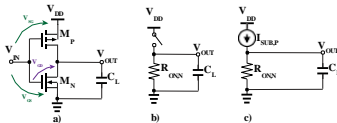
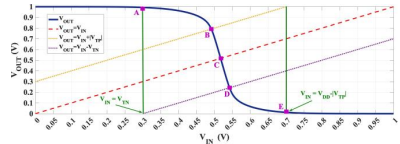


Figure 13: a) CMOS Inverter; b) Equivalent model 5; c) More detailed equivalent model 5



- $V_{IN} > V_{DD} - |V_{TP}|$: M_P is OFF (open switch) and M_N is ON
- $V_{GD,N} > |V_{TN}|$ (area below the purple line) $\rightarrow M_N$ is in triode region, equivalent to $R_{ON,N}$
- The output capacitor, C_L , is discharged through $R_{ON,N}$
- While V_{IN} increases, the sub-threshold leakage current of M_P ($I_{SUB,P}$) stops charging C_L

- $V_{IN} > V_{DD} - |V_{TP}|$: M_P is OFF (open switch) and M_N is ON
- $V_{GD,N} > |V_{TN}|$ (area below the purple line) $\rightarrow M_N$ is in triode region, equivalent to $R_{ON,N}$
- The output capacitor, C_L , is discharged through $R_{ON,N}$
- While V_{IN} increases, the sub-threshold leakage current of M_P ($I_{SUB,P}$) stops charging C_L

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Equations

$$R_{ON,P} = \frac{1}{K_P (W_P/L_P) (V_{SG} - |V_{TP}|)} \quad (1)$$

$$R_{ON,N} = \frac{1}{K_N (W_N/L_N) (V_{GS} - V_{TN})} \quad (2)$$

$$I_{SAT,P} = \frac{K_P}{2} \frac{W_P}{L_P} (V_{SG} - |V_{TP}|)^2 (1 + \lambda_P V_{SD,P}) \quad (3)$$

$$I_{SAT,N} = \frac{K_N}{2} \frac{W_N}{L_N} (V_{GS} - V_{TN})^2 (1 + \lambda_N V_{DS,N}) \quad (4)$$

$$R_{SD,P} = \frac{1}{\lambda_P I_{SAT,P}} \quad (5)$$

$$R_{DS,N} = \frac{1}{\lambda_N I_{SAT,N}} \quad (6)$$