MOS Capacitive Model

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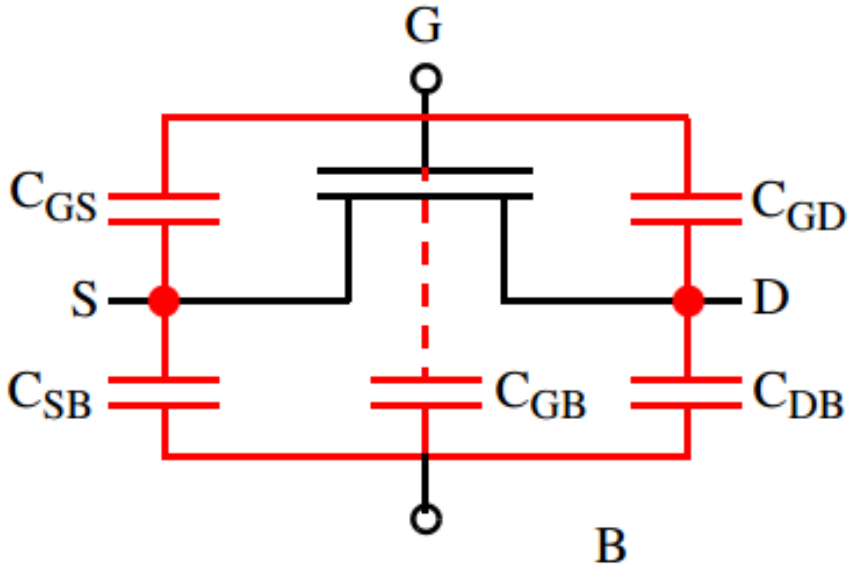


• The dynamic response of a MOSFET transistor is sole function of the time it takes to charge/discharge the parasitic capacitances.

• MOS parasitic capacitances originate from **three sources**:

- the basic MOS structure,
- the channel charge and
- the reverse-biased PN junctions of drain and source.

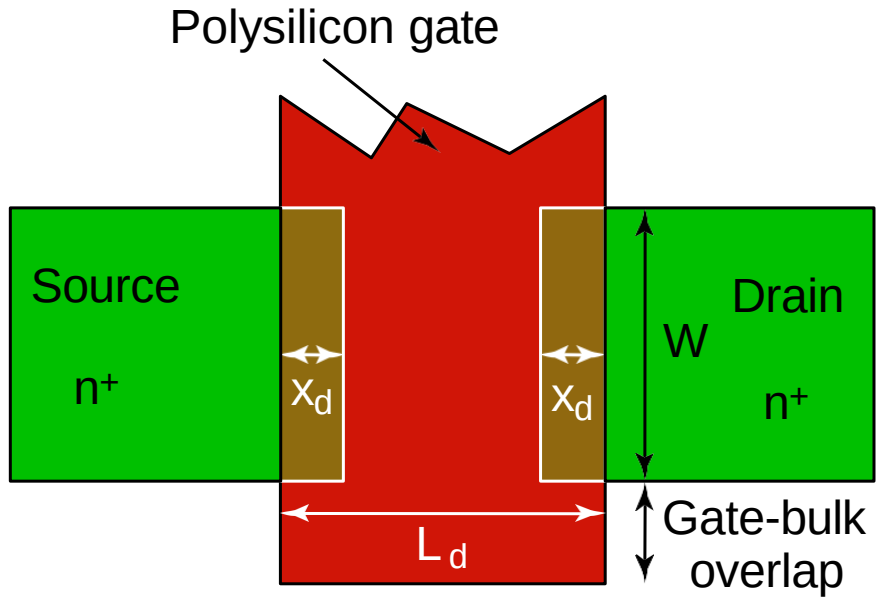
MOS Structure Capacitances

- Both source and drain tend to extend somewhat below the oxide by an amount x_d, called the *lateral diffusion*.
- This overlap is unavoidable and gives rise to a parasitic linear capacitance between gate and source (drain) that is called the *overlap capacitance.*

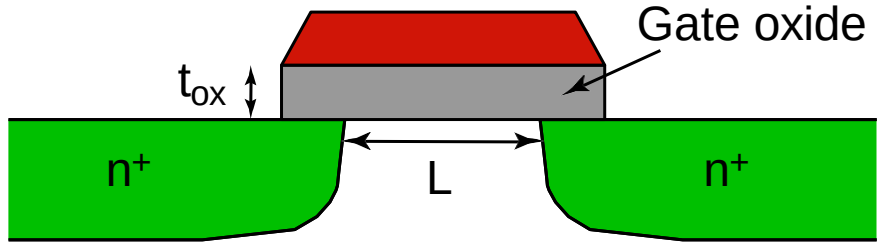
$$c_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Capacitance per unit area

$$C_{gs,ov} = C_{gd,ov} = W x_d c_{ox}$$

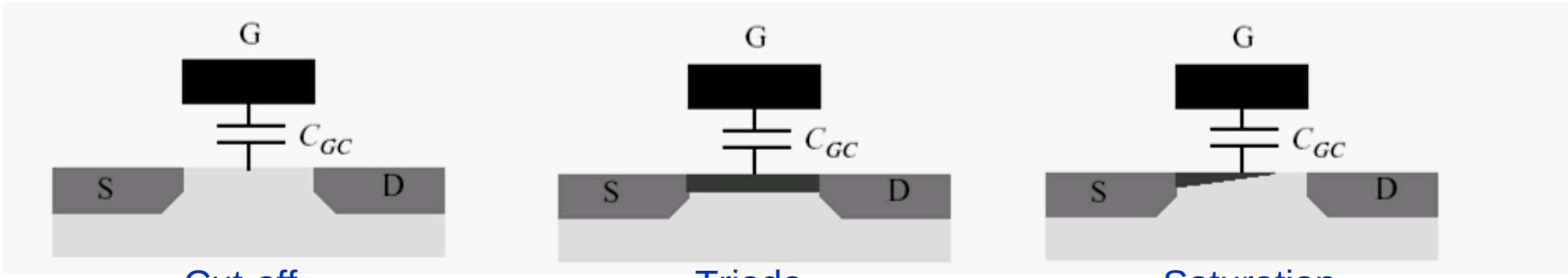


Top view

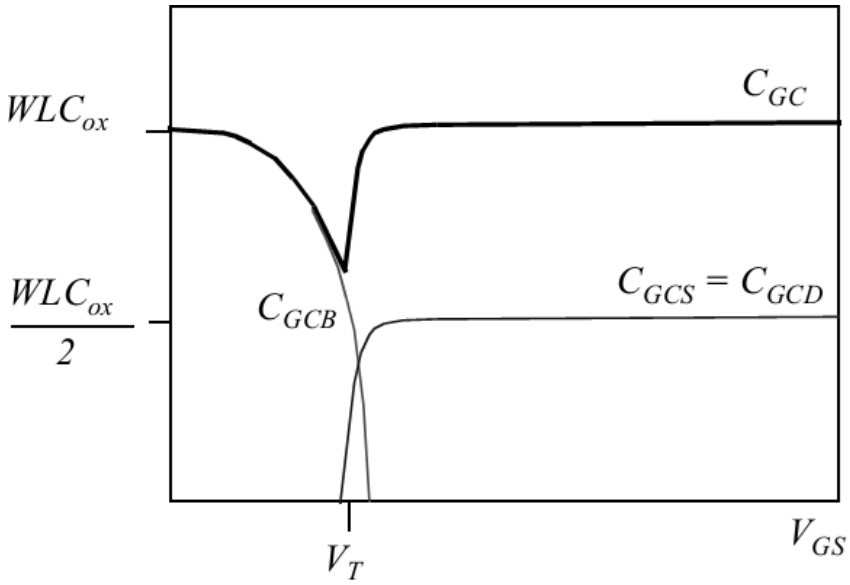


Cross section

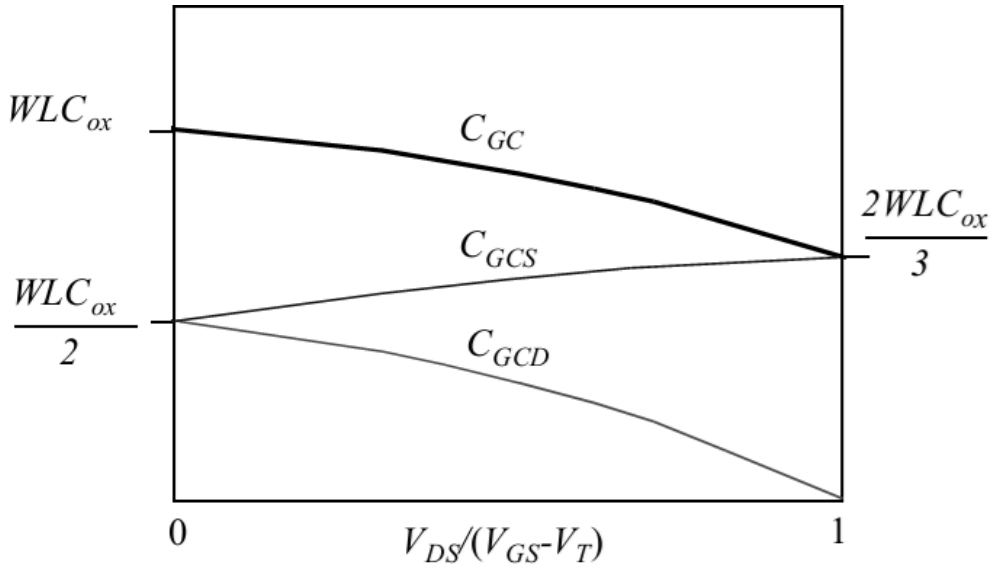
MOS Channel Capacitance



Cut-off Triode Saturation

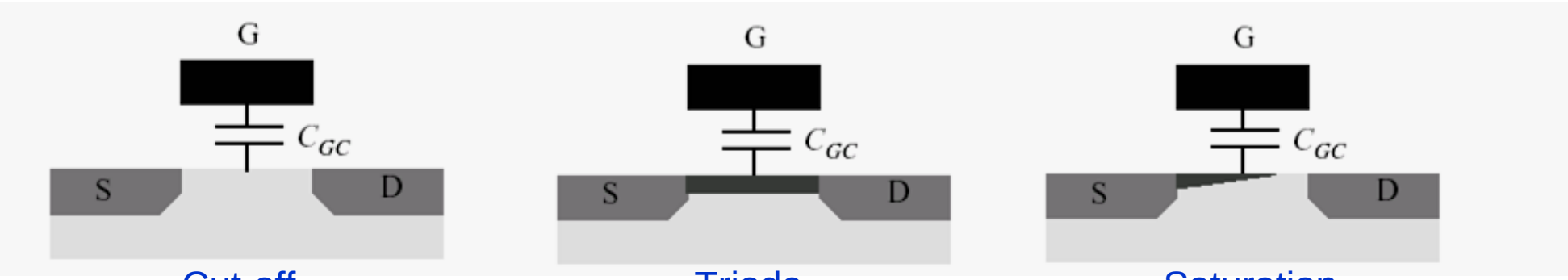


(a) C_{GC} as a function of V_{GS} (with V_{DS}=0)



(b) C_{GC} as a function of the degree of saturation

MOS Channel Capacitance



Cut-off Triode Saturation

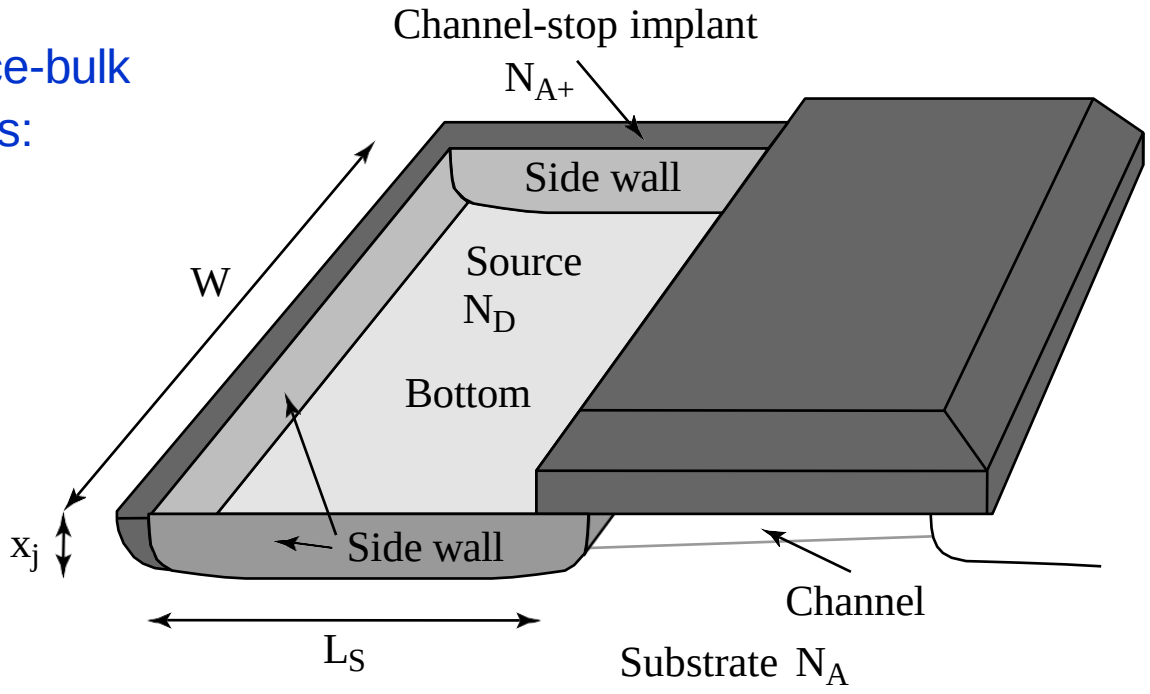
Operation region	C_{gb}	C_{gs}	C_{gd}
Cut-off	$C_{ox}WL$	0	0
Triode	0	$(C_{ox}WL)/2$	$(C_{ox}WL)/2$
Saturation	0	$(2/3)(C_{ox}WL)$	0

- Most important regions in digital design: triode and cut-off

Junction Capacitances

Let us consider the reverse-biased source-bulk *pn* junction. It consists of two components:

- The *bottom-plate* junction, which is formed by the source region and the *p* substrate.
- The *side-wall* junction, formed by the source region and the *p+* channel-stop implant.

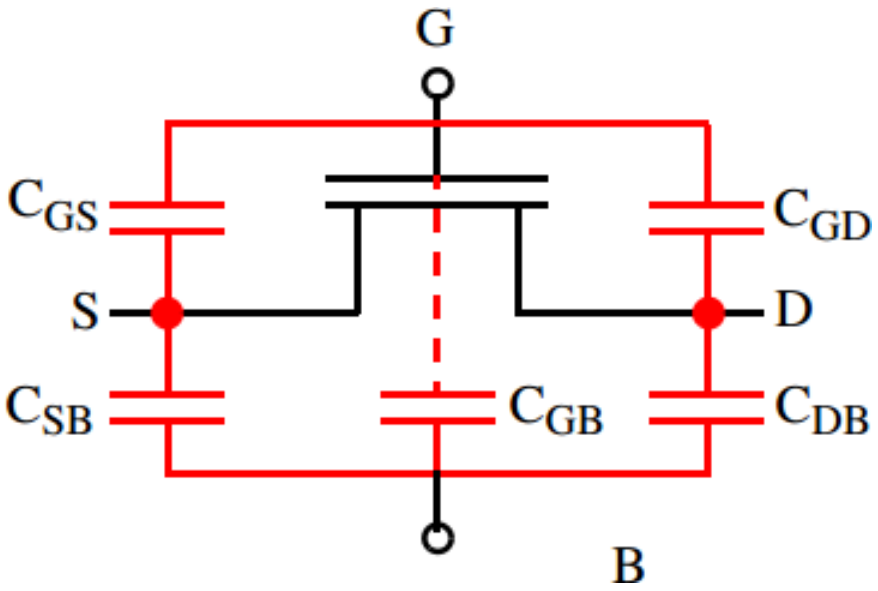


$$C_{jsb,tot} = C_{sbA} \times Area + C_{sbp} \times Perimeter = K_{eq}^{sbA} C_{j0,sbA} W L_S + K_{eq}^{sbp} C_{j0,sbp} (2L_S + W)$$

Similar results can be derived for the drain:

$$C_{jdb,tot} = C_{dbA} \times Area + C_{dbp} \times Perimeter = K_{eq}^{dbA} C_{j0,dbA} W L_S + K_{eq}^{dbp} C_{j0,dbp} (2L_S + W)$$

MOS Capacitive Model



•Aside from the MOS structure capacitances, all capacitors are nonlinear and vary with the applied voltage

$$C_{GD} = C_{gd} + C_{gd,ov}$$

$$C_{GS} = C_{gs} + C_{gs,ov}$$

$$C_{SB} = C_{jsb,tot}$$

$$C_{DB} = C_{jdb,tot}$$

$$C_{GB} = C_{gb}$$

Example

- **Capacitances in 0.25 μm CMOS process**

	C_{ox} (fF/μm²)	C_j (fF/μm²)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	1.9	0.48	0.9	0.22	0.32	0.9

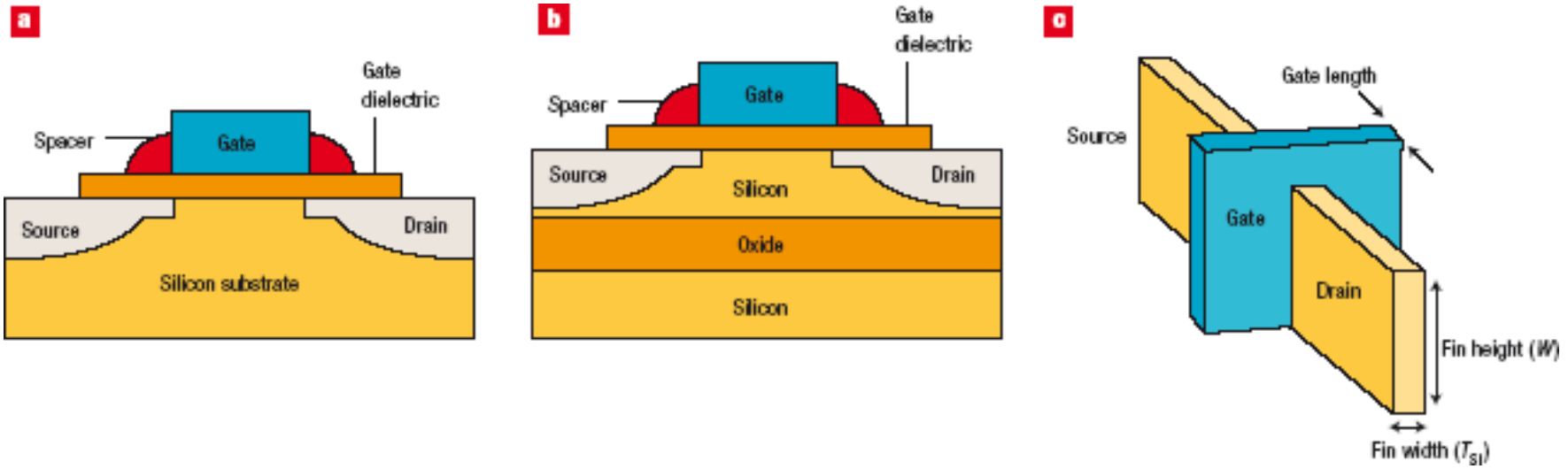
Example: For an NMOS with L = 0.24 μm, W = 0.36 μm, $L_D = L_S = 0.625$ μm, $V_{GS}=0$

$$C_{GS}=C_{GD}=C_{gs,ov} = C_{gd,ov} = C_{ox}\, x_d\, W = 0.11 \text{ fF}$$

$$C_{GB} = C_{ox}\, WL = 0.52 \text{ fF}$$

$$C_{SB}=C_{DB}=C_{jdb,tot}=C_{jsb,tot} = C_{jsbA} = C_j\, L_S\, W + C_{jsw}\,(2L_S + W) = 0.9 \text{ fF}$$

Modern silicon transistors



•**a.** A traditional n-channel MOSFET uses a highly doped n-type polysilicon gate electrode, a highly doped n-type source/drain, a p-type substrate, and a silicon dioxide or oxynitride gate dielectric.

•**b**. A silicon-on-insulator (SOI) MOSFET is similar to the traditional MOSFET except the active silicon is on a thick layer of silicon dioxide. This electrical isolation of the silicon reduces parasitic junction capacitance and improves device performance.

•**c.** A finFET is a three-dimensional version of a MOSFET. The gate electrode wraps around a confined silicon channel providing improved electrostatic control of the channel electrons.

Modern silicon transistors