Towards battery-free and low-cost distributed sensor node: approaches and perspectives

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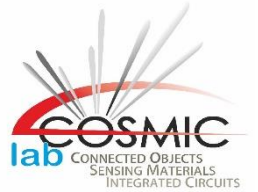


About the speaker

- World-wide experience as a Researcher
  - I have lived in Italy, Netherlands, Australia and Singapore.
- I have earned my technical background in world-wide and well-renewed
  - Universities (UniCT, PoliTO, Monash Uni, UniSyd, UNSW, NUS and now UniGE)
  - R&D institutions (LINK foundation, Turin, Italy and FBK, Trento, Italy)
  - consultant activities (STMicroelectronics)
  - and direct work experiences in semiconductor companies (NXP).

I have been involved into mixed-signal Integrated Circuits design flow
from the ideas conceiving and design
to measurement validation in the lab.

The students will benefit from such gained experience and the related expertise.

Outline

Background and motivations

Few example of novel solutions:

- Wake-up oscillator
- DACs
- Sensor example: CDC

Conclusion

Outline

Background and motivations

Few example of novel solutions:

- Wake-up oscillator
- DACs
- Sensor example: CDC

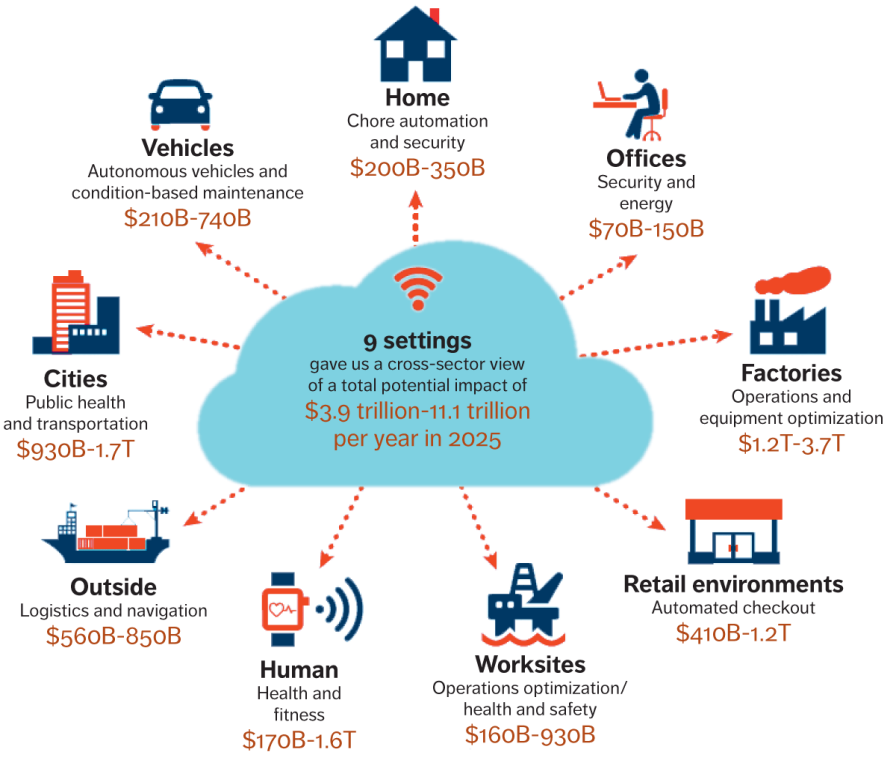
Conclusion

Background and motivations

Energy autonomous systems for distributed sensing and data acquisition imposes stringent constraints on cost, size and power for all on-chip sub-systems

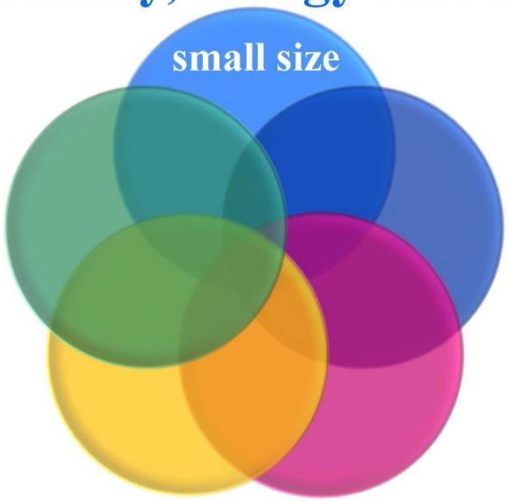
Internet of Things (IoT) is the vision of a world where pervasive integrated electronic systems embedded in everyday life objects are **fully interconnected** to:

- collect,
- process and
- exchange useful information.

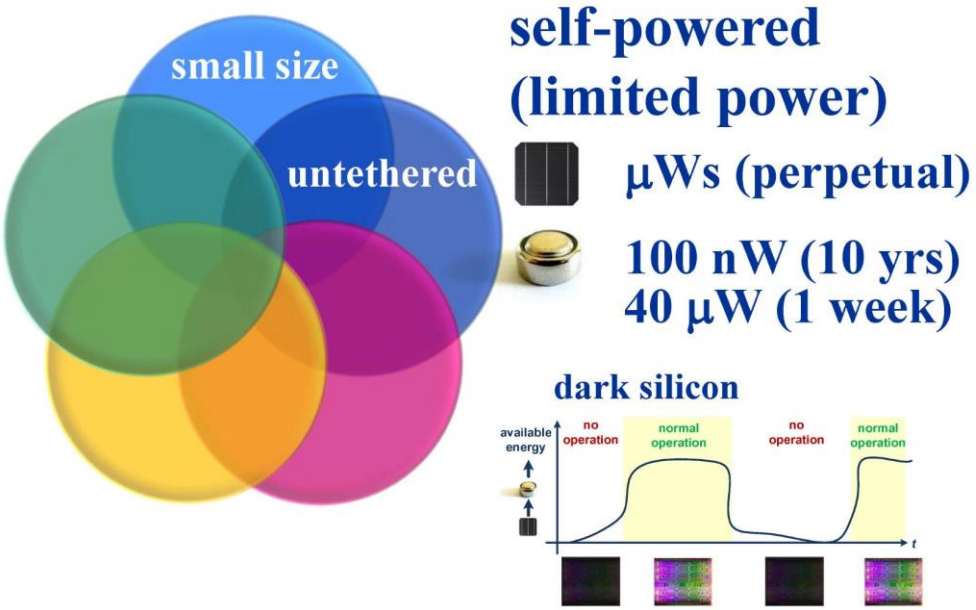


Background and motivations

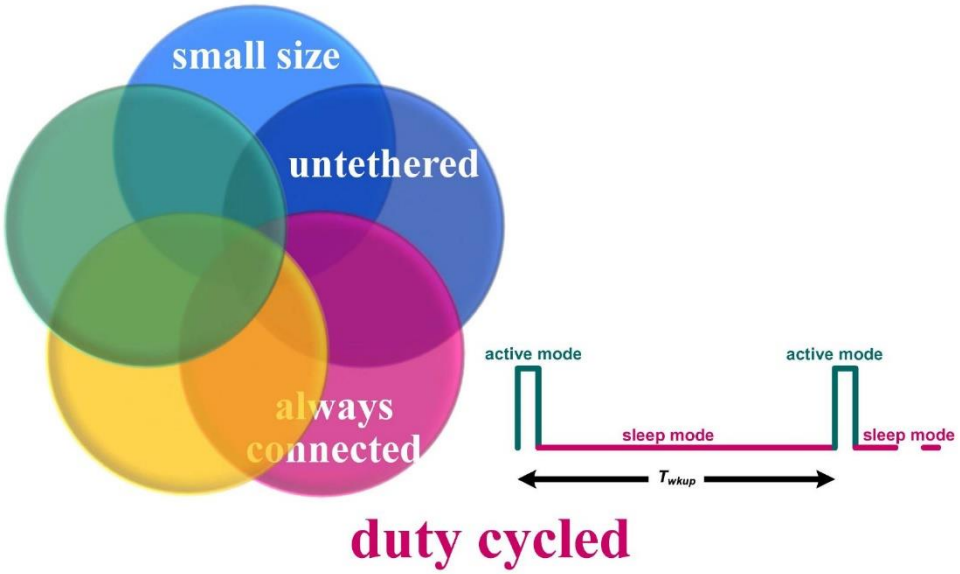
~1-100 mm^3
(battery, energy scavenger)



Background and motivations



Background and motivations



Background and motivations

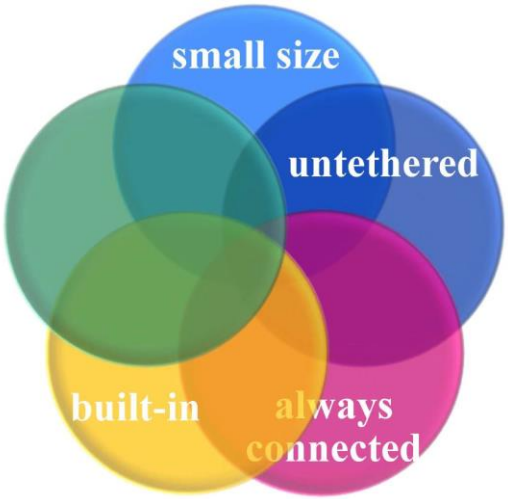
computation

repetitive

- leverage specialized HW

- real time: scalable performance is needed

- data logging: less performance, but memory cost



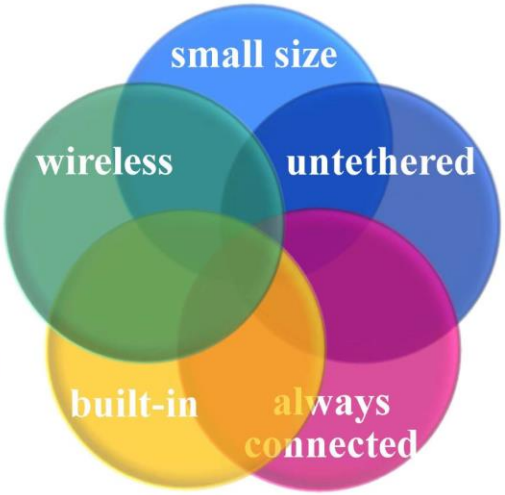
Background and motivations

communication

computation vs communication tradeoff

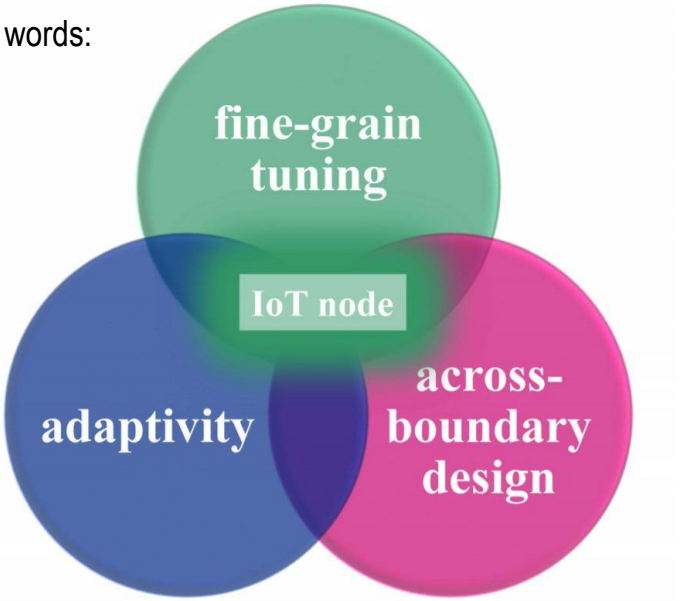
- data representation (compressive sensing, compression)

- limit TX to critical events or significant changes (critical event monitoring)



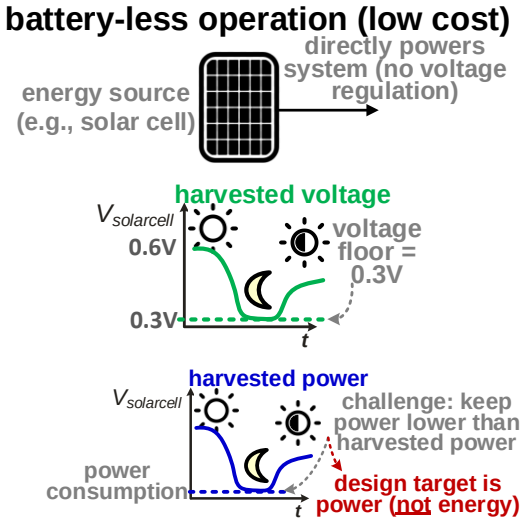
Background and motivations

But also and /or in other words:



How to address these requirements leading to energy autonomous systems?

Background and motivations



No state-of-the art performance are needed.

Priorities to Energy autonomous systems are:

a) low power consumption to last longer

→being powered by harvesters and

→with relaxed specs

- Hundreds of kS/s
- Medium-low resolution (8bit → 12bit)

  new ICs solutions reducing static power consumption
- more digital counterparts

b) low cost to have IoT nodes everywhere

increase automation ←→ reduce human-desing effort

reduced Si area

c) be powered by harvesters to be without bulky batteries

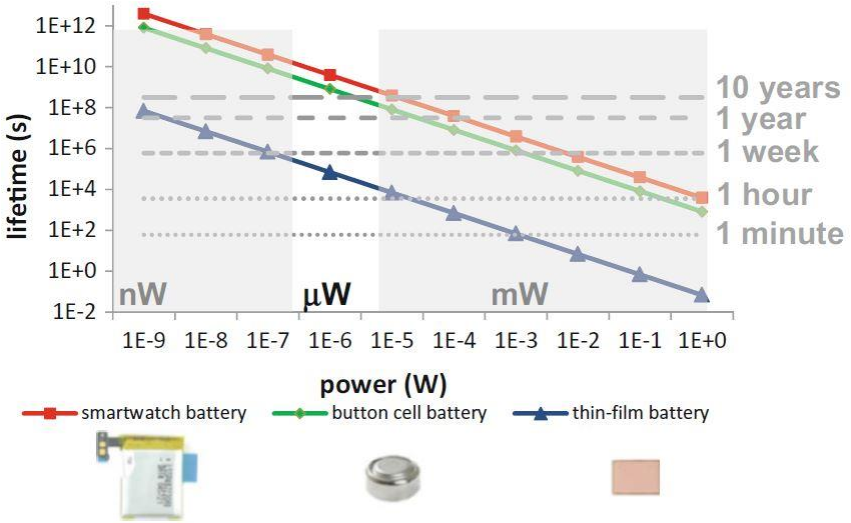
increase batteryless ←→ smaller volume, more integration

Power Consumption VS Battery

Needs for low power consumption arises because of:

- increasing number of connected devices
- intrinsic energy constraint of IoT nodes.

$$t_{lifetime} = \frac{E_{battery}}{P_{avg}}$$



Long lifetime is related with:

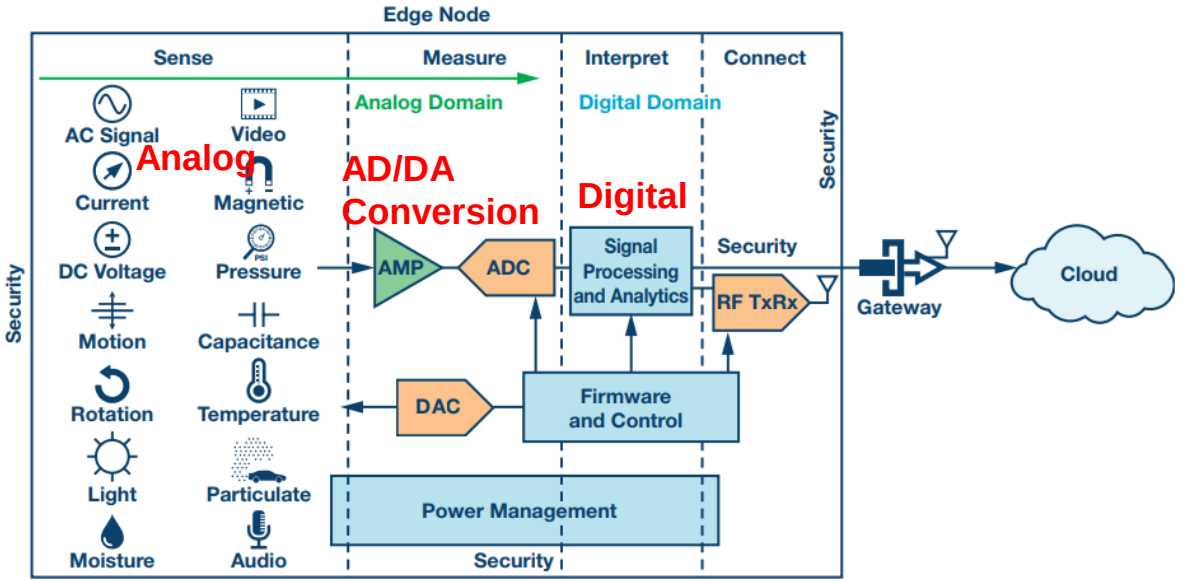
- low voltage,
- low energy
- and size constraints.

type	cost	capacity	volume	energy density
GH43-03992A	30$	300 mAh	2,400mm^3	0.12 mAh/mm^3
LR44	<1$	150 mAh (nonrechargeable)	500mm^3	0.28 mAh/mm^3
Cymbet CBC005	0.2$	5 mAh	0.7mm^3	6.5 mAh/mm^3

M. Alioto (Ed.), Enabling the Internet of Things from Integrated Circuits to Integrated Systems, Springer, 2017.

Background and motivations

General architecture



Ian Beavers. *Intelligence at the Edge Part 1: The Edge Node*. [Online]: https://www.analog.com/en/technical-articles/intelligence-at-the-edge-part-1-the-edge-node.html

Every information coming from the sensing devices undergoes the conversion process:
Surrounding **Analog** environment → physical signal → **Digital** signal → data

The reverse process happens for each operation which needs to act to the world:
Digital signal → Control signal → Thing operation

Strong interest for mostly digital analog/mixed signal blocks

Background and motivations

- Ad-hoc Software approach
  - The CRAFT program seeks to **shorten the design cycle** for custom integrated circuits to months rather than years be means of a **software-based SoC generator** [DARPA].
  - Python-based tool that interfaces with the Cadence Virtuoso software.
    (open-source framework named **Berkeley Analog Generator (BAG)** [BAG19]).
    This approach relies on “analog-based” design.
    Any transistor’s size comes from an **iterative process**

→**IC designers** require **additional competencies** and effort to exploit such generators.

- Fully synthesizable digital (automated) design exploiting existing tool
  - This approach relies on existing and well-known digital (automated) design tools.
    Layout comes from an automated design flow:
    from Verilog code to layout in 1 day working for each process design kit

→**IC designers** use their own digital design skills (no further learning effort for other ad-hoc software)

[DARPA] DARPA program “Circuit Realization at Faster Timescales(CRAFT)” website – Available at https://www.darpa.mil/program/circuit-realization-at-faster-timescales.

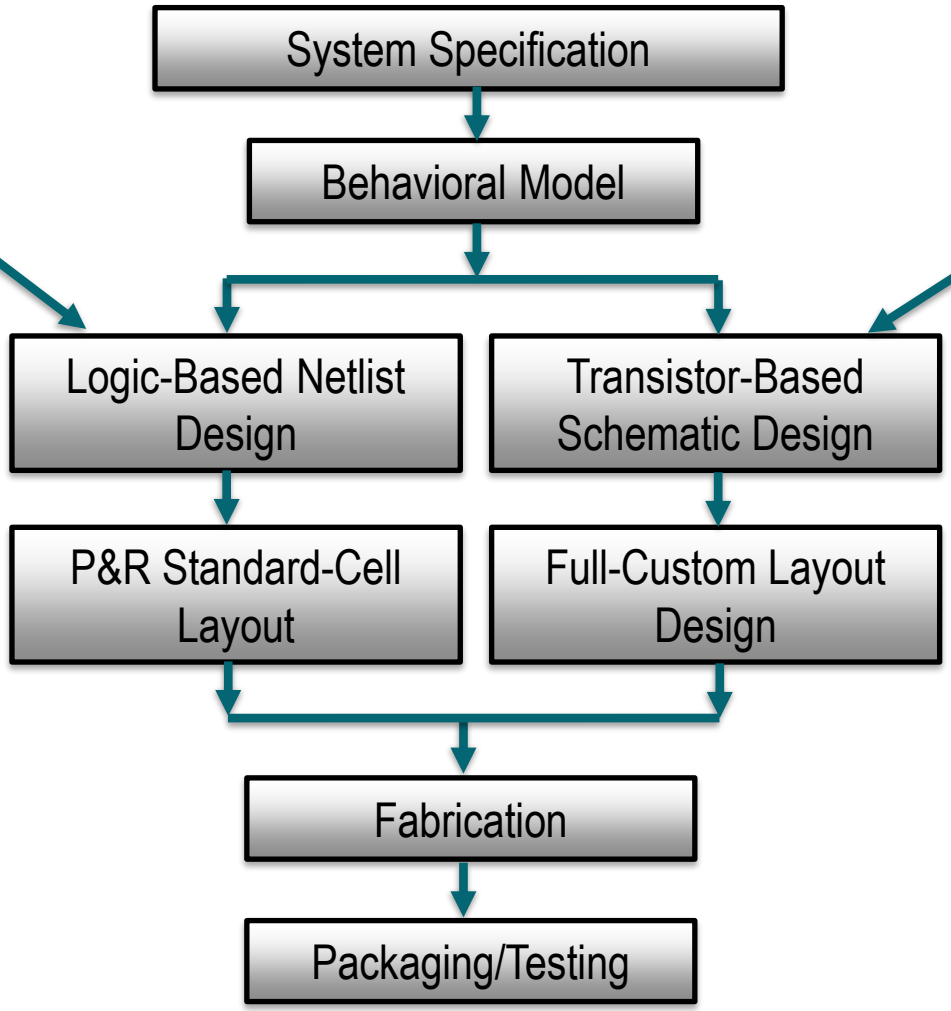
[BAG19] E. Chang, N. Narevsky, K. Settaluri, E. Alon, BAG: A Process-Portable Framework for Generator based AMS Circuit Design, Proc. of 2019 IEEE Custom Integrated Circuits Conference (CICC)

[ULPIoT] MSCA-IF-GF program “Ultra-Low Power and Highly-Scalable Interfaces for the Internet of Things (ULPIoT)” website – Available at https://cordis.europa.eu/project/rcn/206710/factsheet/en

Research Motivation

Digital VS analog Design Flow

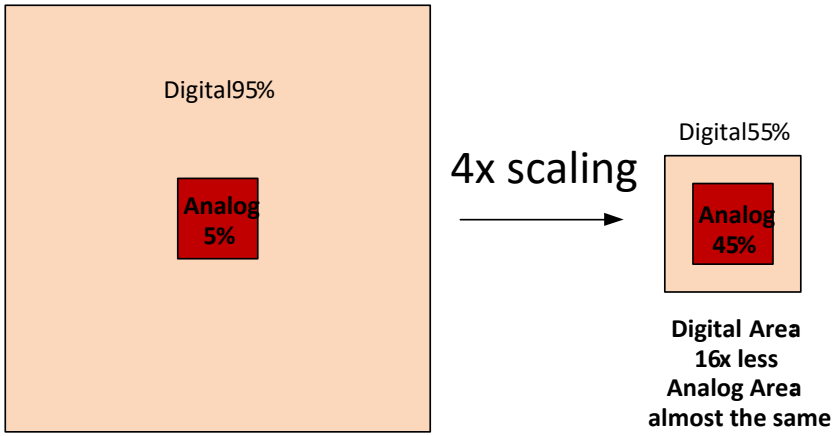
Digital Design Flow:
- Automatic
- Portability
- Time-to-market
- Reasonable performance

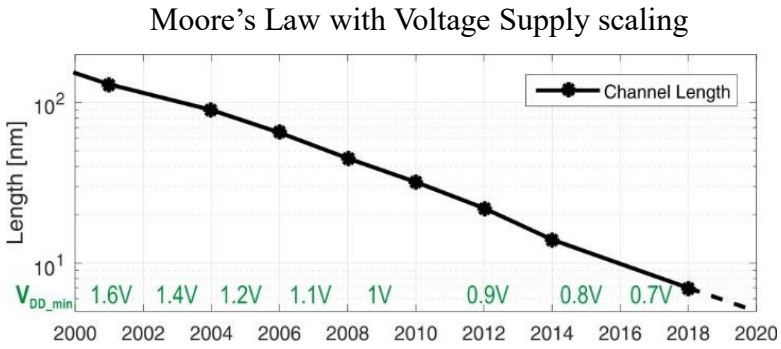


Analog Design Flow:
- Longest design time
- Manual layout
- Labor intensive
- Highest performance

Research Motivation

analog/mixed signal	fully/mostly digital
custom, time-consuming	fully automated (stdcell)
poor $g_m r_0$ in recent CMOS generations, mismatch is a challenge	robust against process variations
above- or near-threshold V_{DD} (MOS biasing, SNR)	operation down to deep subthreshold
area does not really scale with technology	takes advantage of technology scaling





Analog design challenges:

- reduced signal swing,
- worse matching
- No benefit from scaling
-poor "analog" characteristics of nanoscale transistors.

Strong interest for mostly digital analog/mixed signal blocks

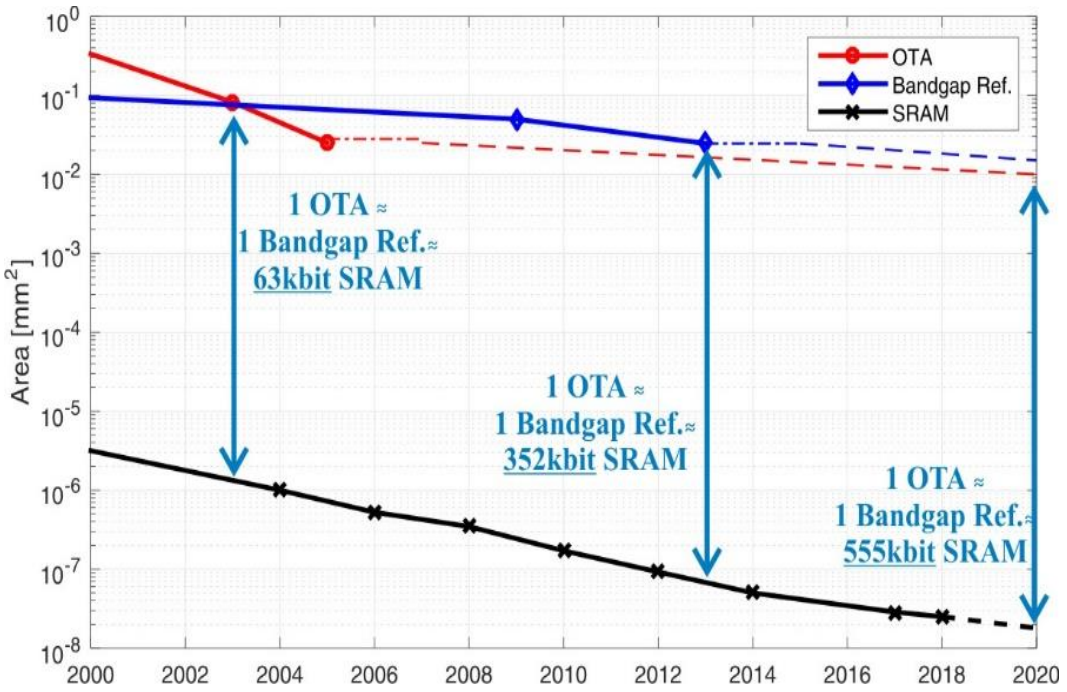
Research Motivation

Analog fundamental building blocks such as **Operational Transconductance Amplifier (OTA)** and **Bandgap Reference**, have been negligibly affected by the technology scaling.
On the contrary digital blocks like **SRAM** have continuously benefited from technological advances.

In ten years, the same analog function is implemented in an area in which the number of digital building blocks that can be placed is more than **5x the number of blocks that were placed a decade before** (from 63 kbit of SRAM in 2003 to 352 kbit in 2013)

Phone's Improvements of Performance/Battery-Capacity/ Thickness

	2009	2014	Yearly changes
Computational Performance (Normalized)	1	57	125%
Tickness	12.5mm	~8mm	-7%
Battery Capability	1500mAh	2800mAh	10%

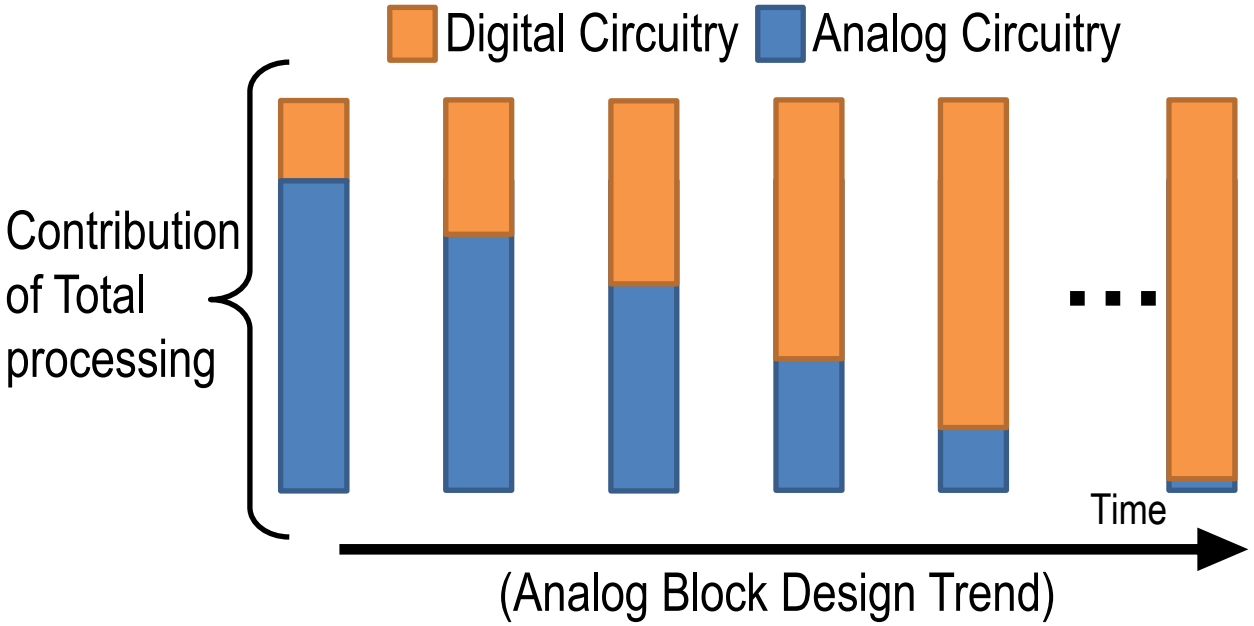


Scaling of Analog ICs blocks as Operational Transconductance Amplifier (OTA), Bandgap and Digital ICs blocks as bit size of SRAM

Research Motivation

Digital (Automated) ICs design

- **Increasing trend** in finding alternative IC design strategies **to implement analog functions exploiting digital-in-concept design methodologies**.
- Exploit existing tools
- Reduced human-design effort
- Voltage and technology scalability



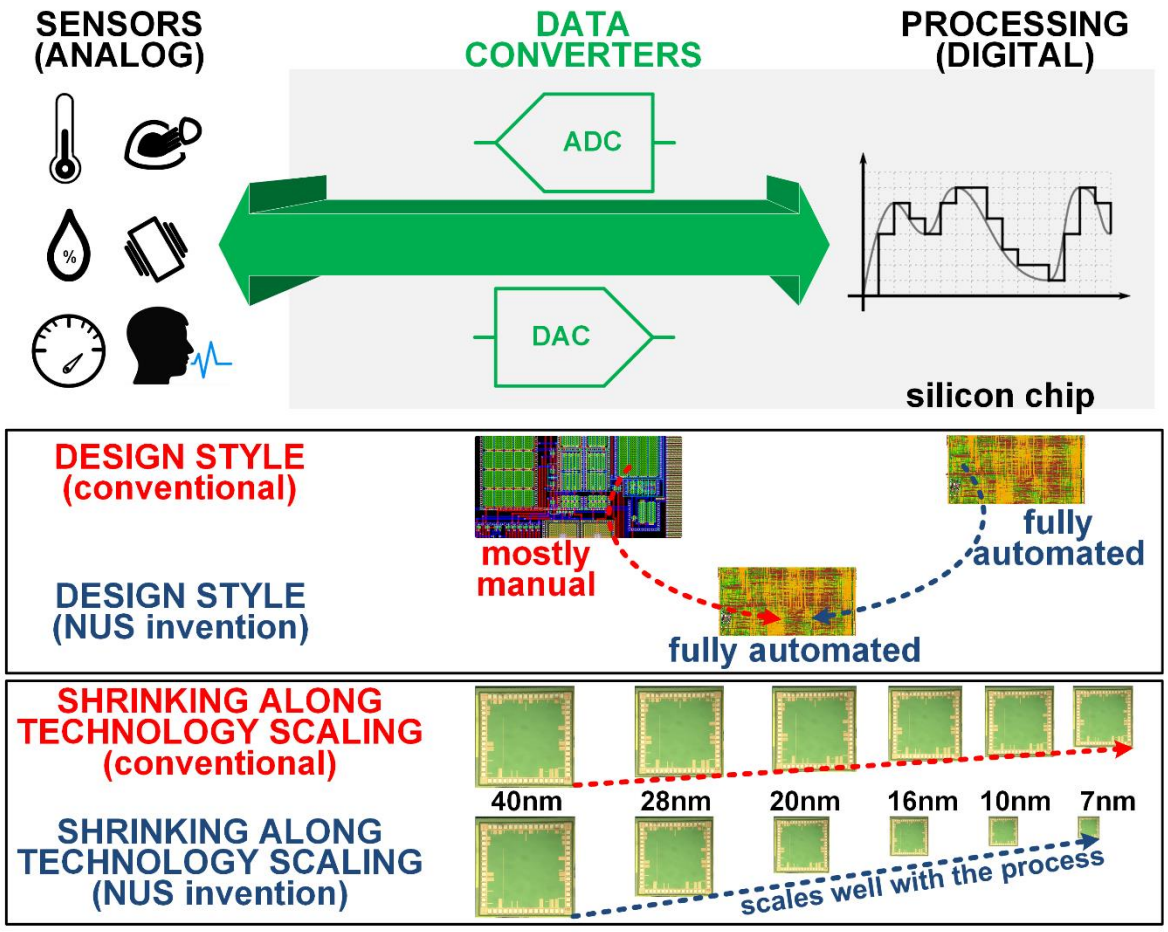
Research Motivation

Digital (Automated) ICs design

A digital nature allows a design with very low effort (e.g., in Verilog) and fully-automated digital flows.

- Why Fully Synthesizable?
  - → Technology and design Portability between different technology nodes:
    - →Just changing the Process Design Kit (PDK)
    - →Re-using the same Verilog code
- Target:
  - Low cost (low design effort, technological portable, skinking with the technology)
  - LoW power consumption
    - Battery-les system or powered by harvester
    - Performance
      - Almost Independent with the supply voltage or
      - With graceful degradation of the performance lowering the supply voltage

Research achievements



Research achievements

I worked to develop innovative ideas on

- mostly/fully-synthesizable,
- highly-scalable,
- technology portable,
- Ultra low power and energy-efficient ICs for the Internet of Things Era

ICs cell I have been propose in the literature:

Fully Synthesizable Wake-up oscillator

Fully Synthesizable DACs: 14-bit and 16-bit (differential)

Fully synthesizable ADC

Fully synthesizable Comparator

Fully digital OTA

Fully synthesizable Capacitive-to-digital Converter

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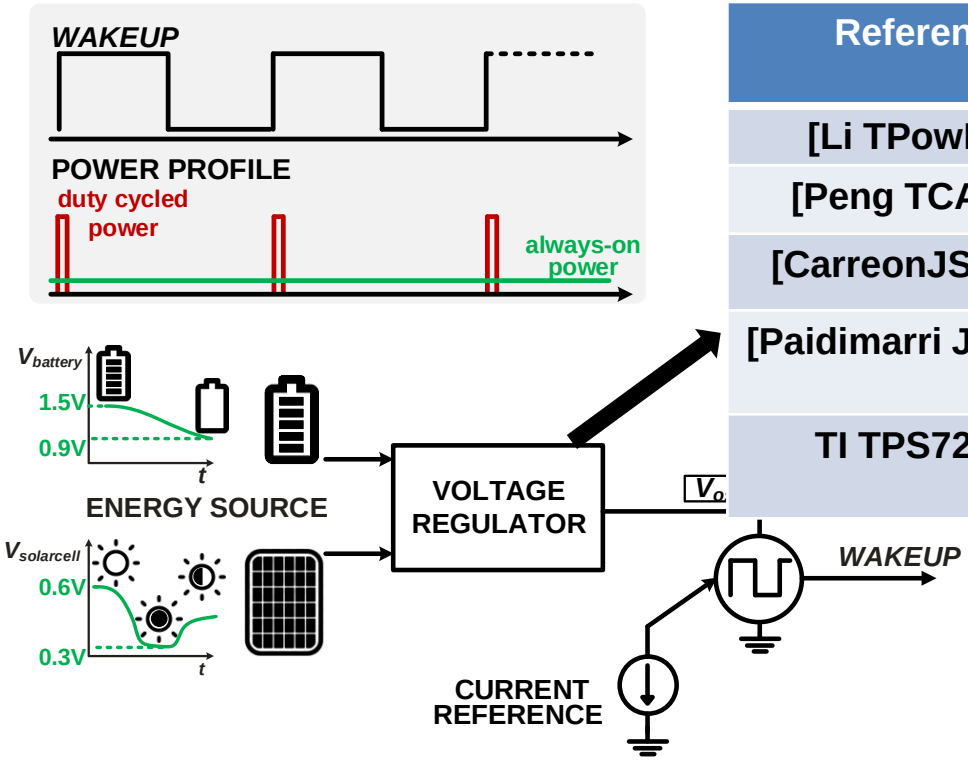
- DACs
- Sensor example: CDC

Conclusion

Wake-up oscillator: motivation

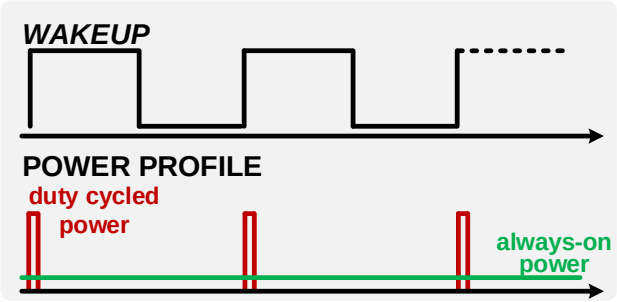
Wake-up oscillator for duty-cycled operation of IoT nodes

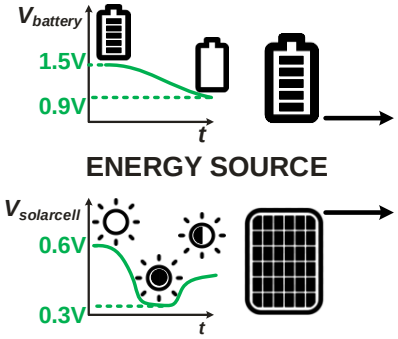


Reference	Type	Fully on chip	Quiescent Power
[Li TPowE16]	Digital LDO	Yes	>4µW
[Peng TCAS17]	Analog LDO	Yes	>350nW
[CarreonJSSC16]	Digital LDO	Yes	>1.18µW
[Paidimarri JSSC17]	Switching (Buck)	No	0.5nW
TI TPS72736	Switching (Buck)	No	760nW

Wake-up oscillator: motivation

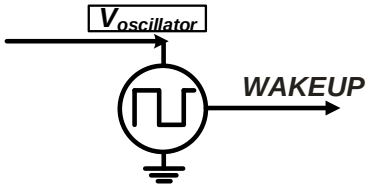
Targeted regulator-less architecture





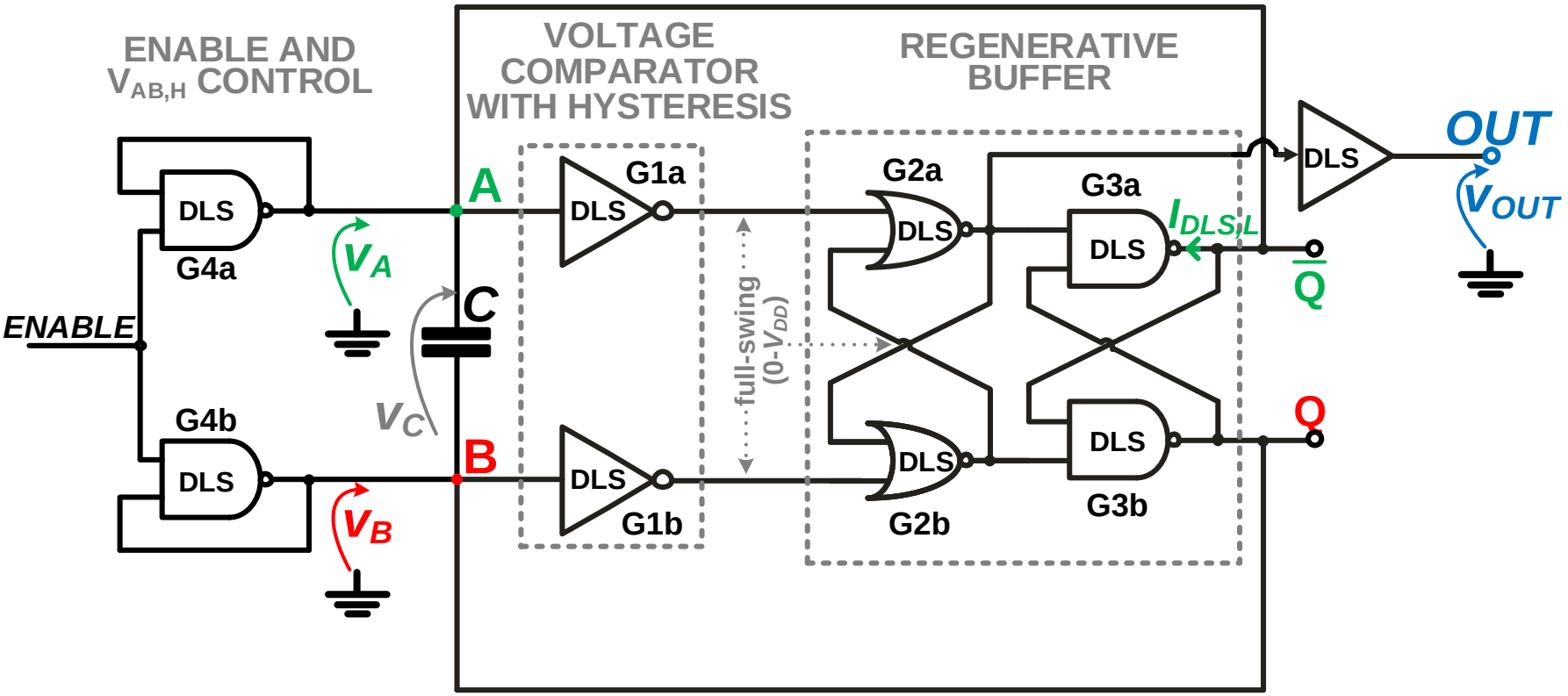
Always on → Need to be very low power
→No Voltage ref. and Current source

Challenge: low oscillation frequency sensitivity to power supply



Wake-up oscillator

Gate-level architecture of the proposed wake-up oscillator

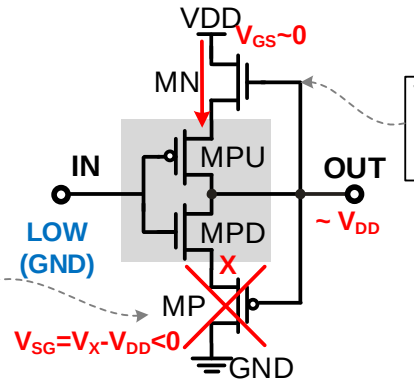


DLS Logic Inverter: the high and low output state

"Dynamic Leakage Suppression" (DLS [Lim15]) Logic also known as "Ultra Low Power" (ULP [Bol07]) Logic

At hIgh output state:

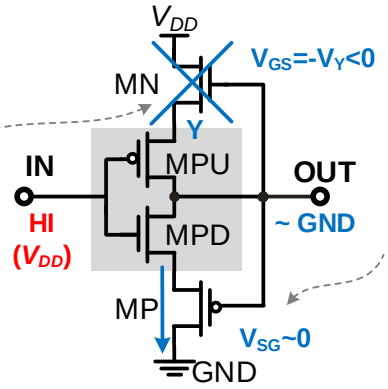
Leakage power dramatically reduced by **MP** biased with $V_{SG}<0$ in series with the **MPD pull-down network**



Very low **MPU current** limited by MN

At low output state:

Leakage power dramatically reduced by **MN** biased with $V_{GS}<0$ in series with the **MPU pull-up network**

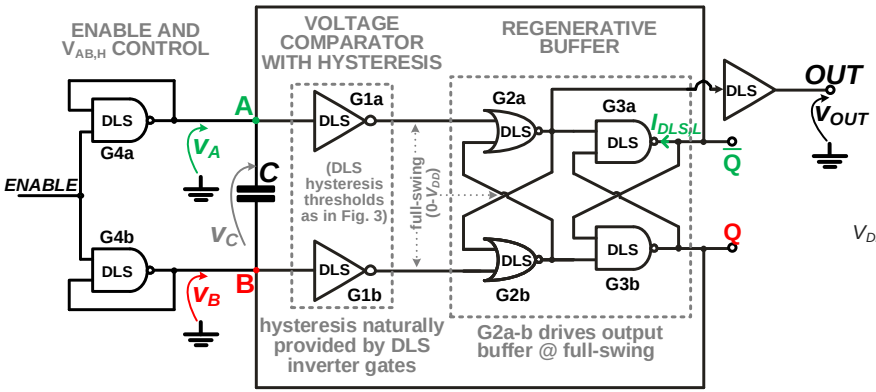


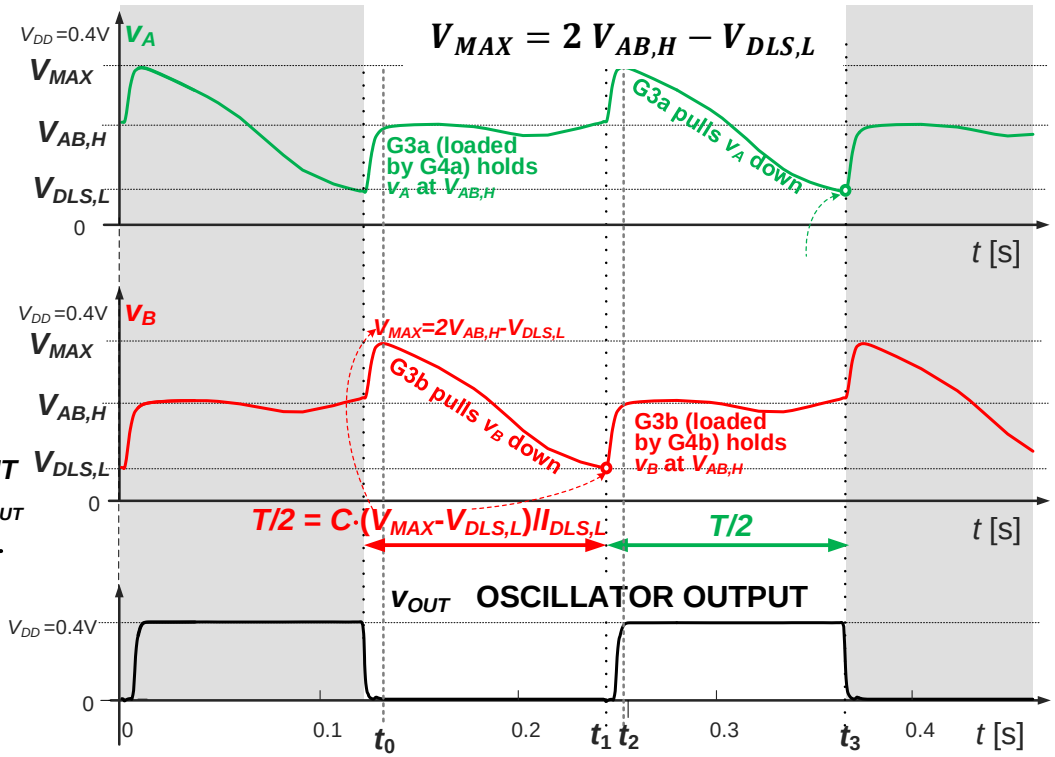
Very low **MPD current** limited by MP

Waveforms

- Frequency oscillation nearly independent of VDD because of $V_{DLS,L}$ and $V_{AB,H}$
- Architecture symmetric but no differential

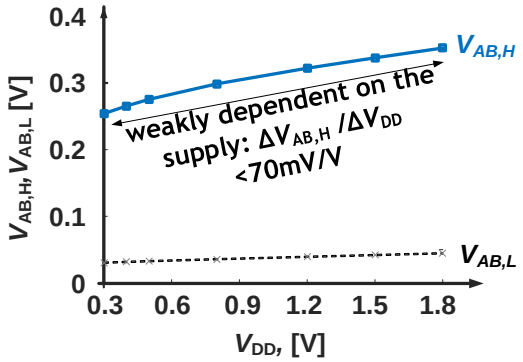
$$T = 2\left(\frac{C\left(V_{MAX} - V_{DLS,L}\right)}{I_{DLS}}\right) + 2t_D$$



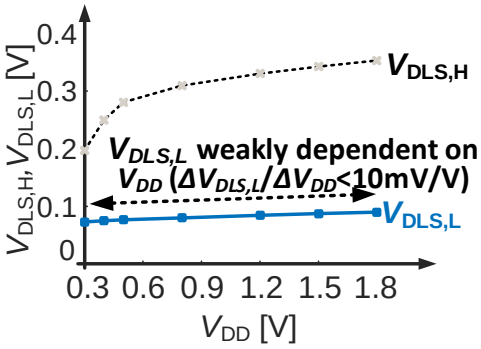


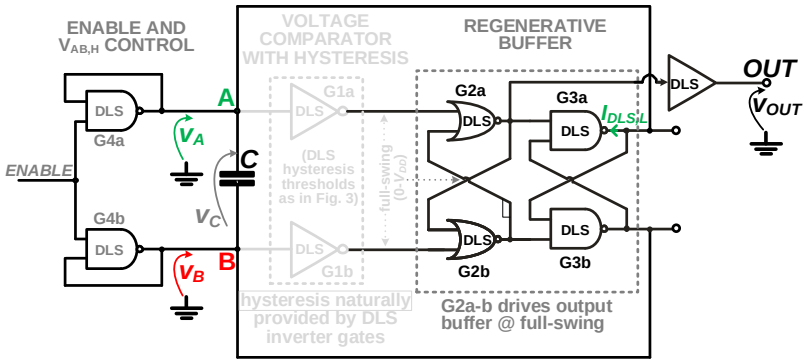
DLS Relaxation Oscillator Operation

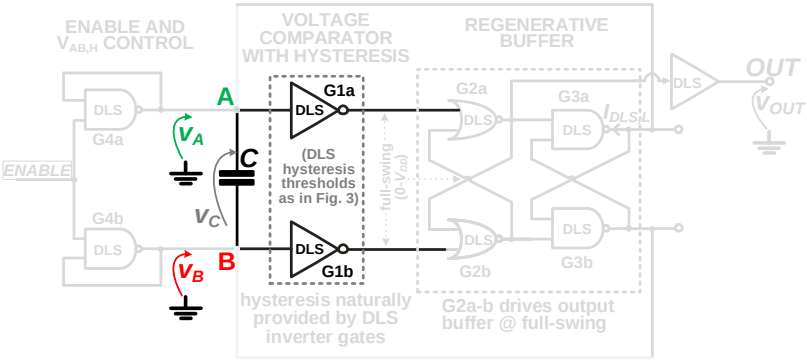
- same for high hyst. threshold of latch with active load
- low threshold of inverter nearly independent of VDD



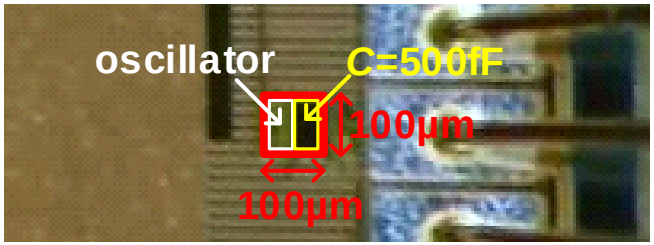
$$T = 2\left(\frac{4C\left(V_{AB,H} - V_{DLS,L}\right)}{I_{DLS}}\right)$$

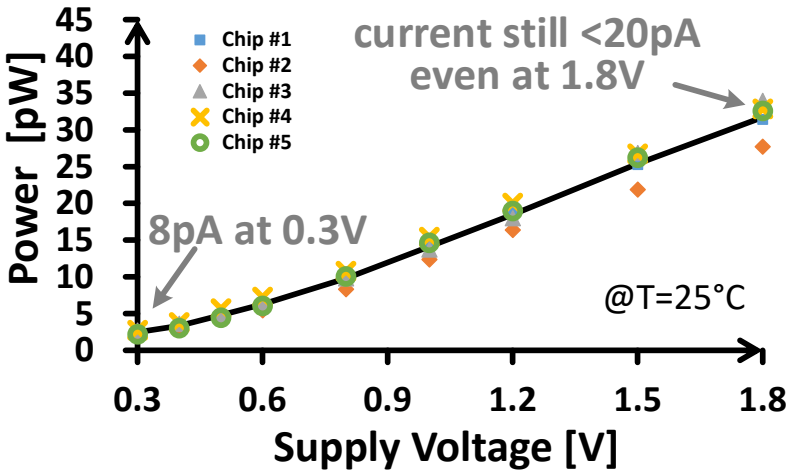


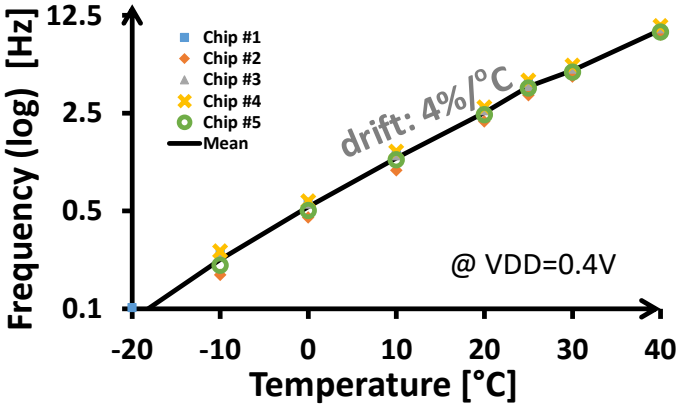


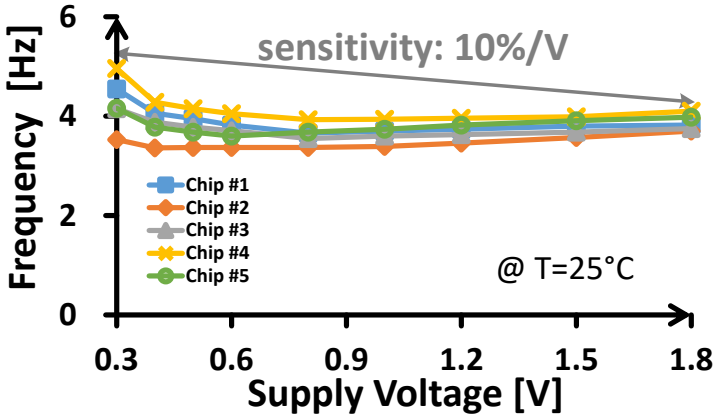


Measurement Results









Outline

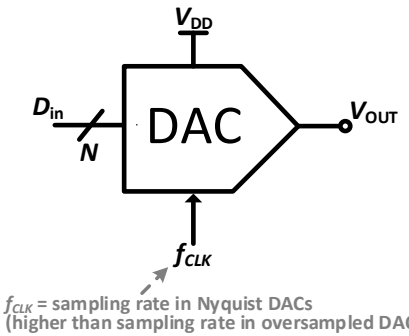
Background and motivations

Few example of novel solutions:

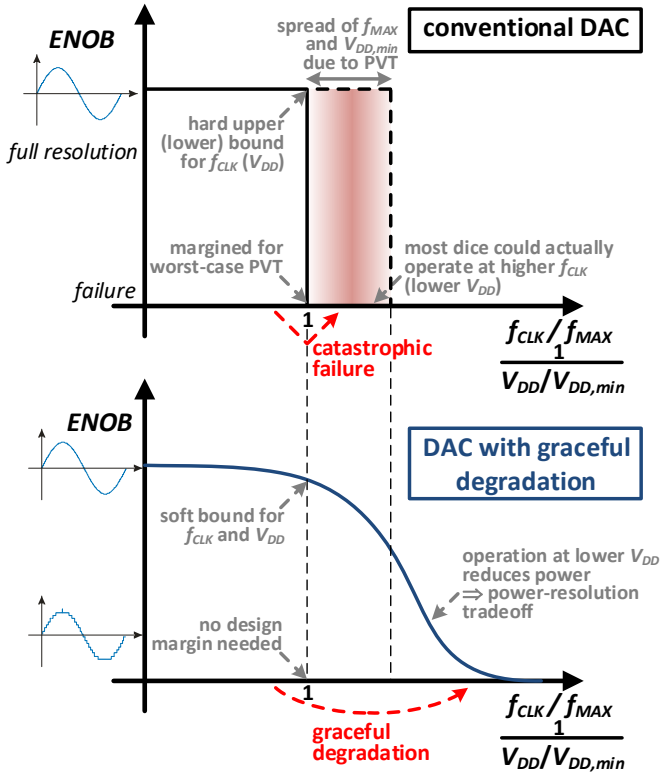
- Wake-up oscillator
- DACs
- Sensor example: CDC

Conclusion

Using Dyadic Digital Pulse Modulation to have graceful degradation of the performance over the supply voltage



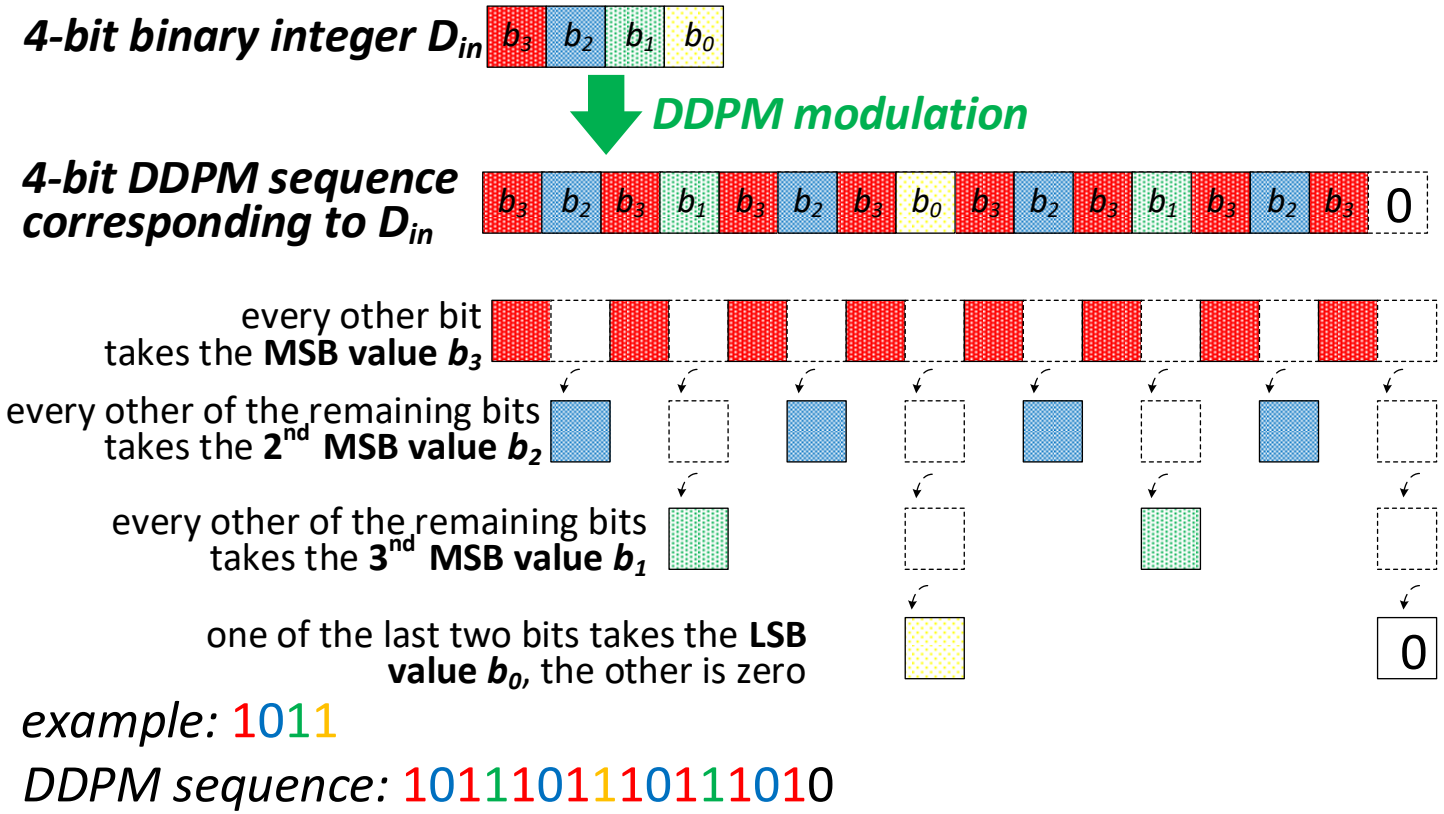
	conventional DAC	DAC with graceful degradation
design margin	worst-case PVT	no margin (design at TT corner)
operation at $V_{DD} < V_{DD,min}$ (design target)	not allowed	allowed (at degraded ENOB)
operation at $f_{CLK} > f_{MAX}$ (design target)	not allowed	allowed (at degraded ENOB)
dynamic energy-resolution tradeoff	NO	YES (at degraded ENOB)



DAC with graceful degradation allows operation at lower voltage and higher frequency than the design target, eliminating the need for PVT design margin, allowing dynamic power-resolution tradeoff via voltage/frequency scaling, and maintaining correct operation even under significant PVT variations (e.g., substantial voltage reduction due to inadequate harvested power, or on-chip oscillator frequency deviations).

• **O. Aiello**, P.Crovetti, M. Alioto, "Fully Synthesizable Low-Area Digital-to-Analog Converter with Graceful Degradation and Dynamic Power-Resolution Scaling", IEEE Transaction on Circuits and Systems I, Vol. 66, Issue 8. p. 2865- 2875, August 2019, doi: 10.1109/TCSI.2019.2903464

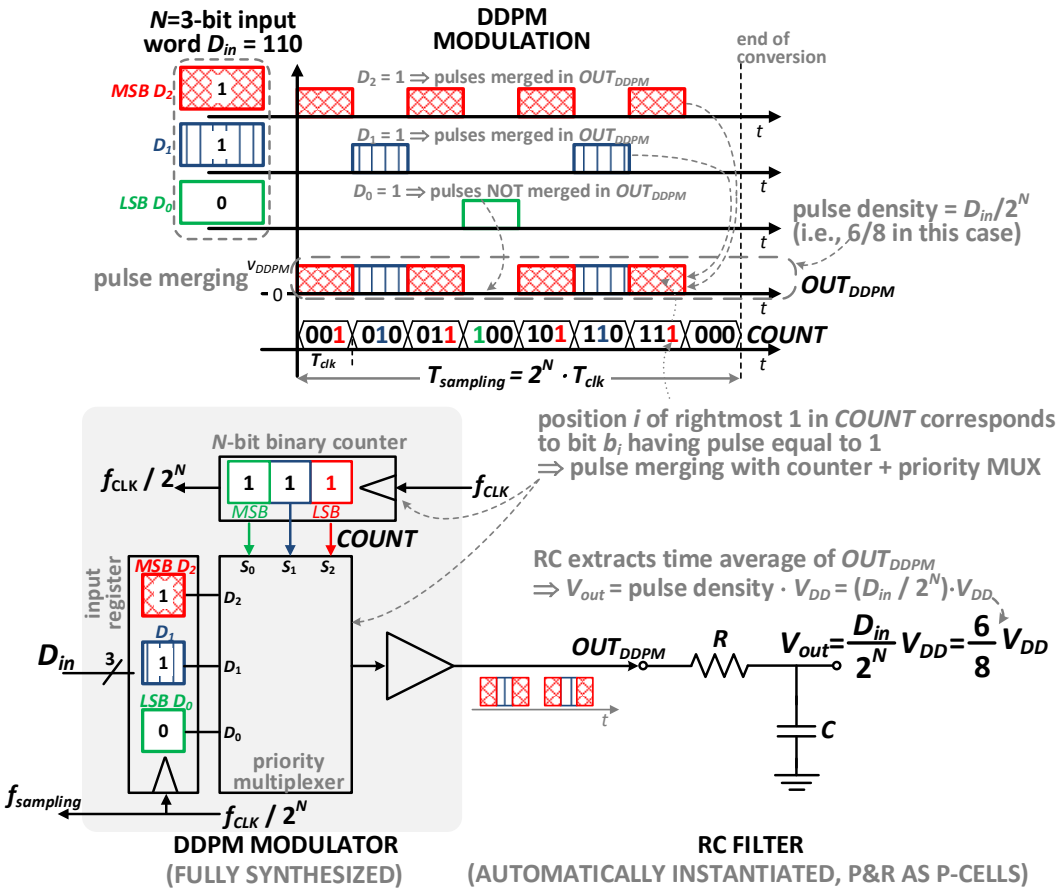
HOW: using Dyadic Digital Pulse Modulation



example: 1011

DDPM sequence: 10111011101110 10

• **O. Aiello**, P.Crovetti, M. Alioto, "Fully Synthesizable Low-Area Digital-to-Analog Converter with Graceful Degradation and Dynamic Power-Resolution Scaling", IEEE Transaction on Circuits and Systems I, Vol. 66, Issue 8. p. 2865- 2875, August 2019, doi: 10.1109/TCSI.2019.2903464

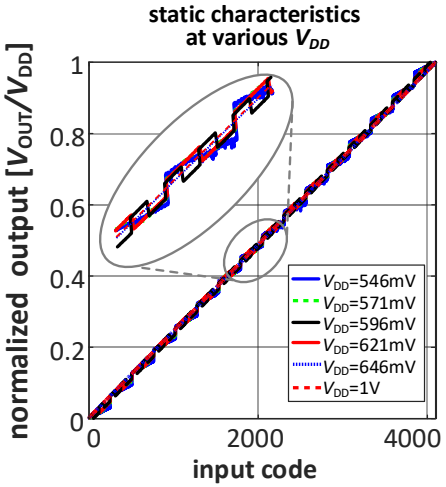


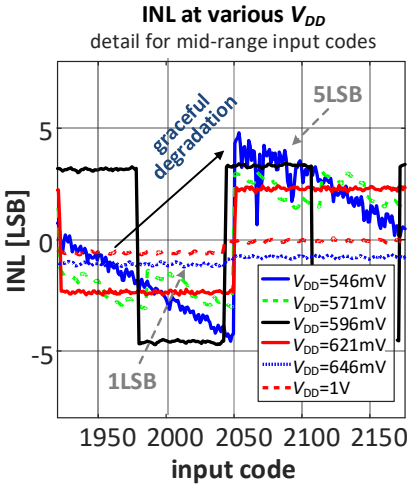
Critical paths showing that the first paths experiencing timing failure are associated with LSBs

• **O. Aiello**, P.Crovetti, M. Alioto, "Fully Synthesizable Low-Area Digital-to-Analog Converter with Graceful Degradation and Dynamic Power-Resolution Scaling", IEEE Transaction on Circuits and Systems I, Vol. 66, Issue 8. p. 2865- 2875, August 2019, doi: 10.1109/TCSI.2019.2903464

Graceful resolution degradation for voltage below (frequency beyond)

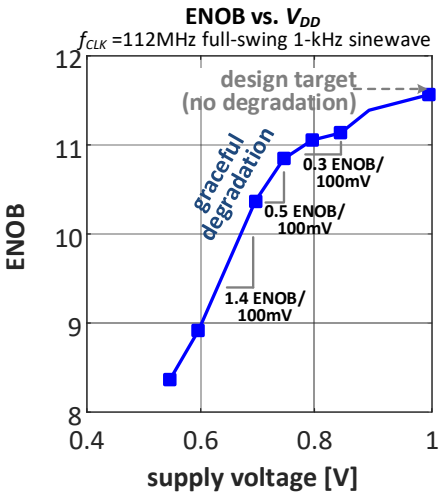
Static characteristics

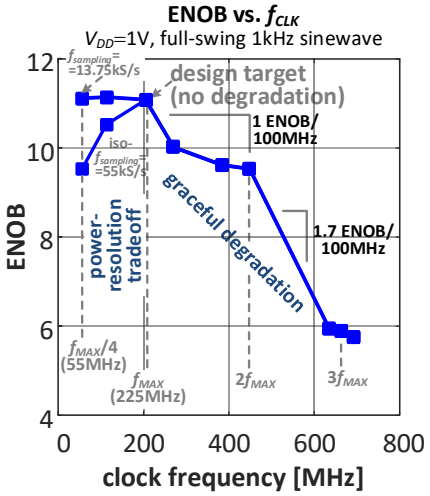




INL

ENOB vs. V_{DD}





ENOB vs. f_{CLK}

• **O. Aiello**, P.Crovetti, M. Alioto, "Fully Synthesizable Low-Area Digital-to-Analog Converter with Graceful Degradation and Dynamic Power-Resolution Scaling", IEEE Transaction on Circuits and Systems I, Vol. 66, Issue 8. p. 2865- 2875, August 2019, doi: 10.1109/TCSI.2019.2903464

Outline

Background and motivations

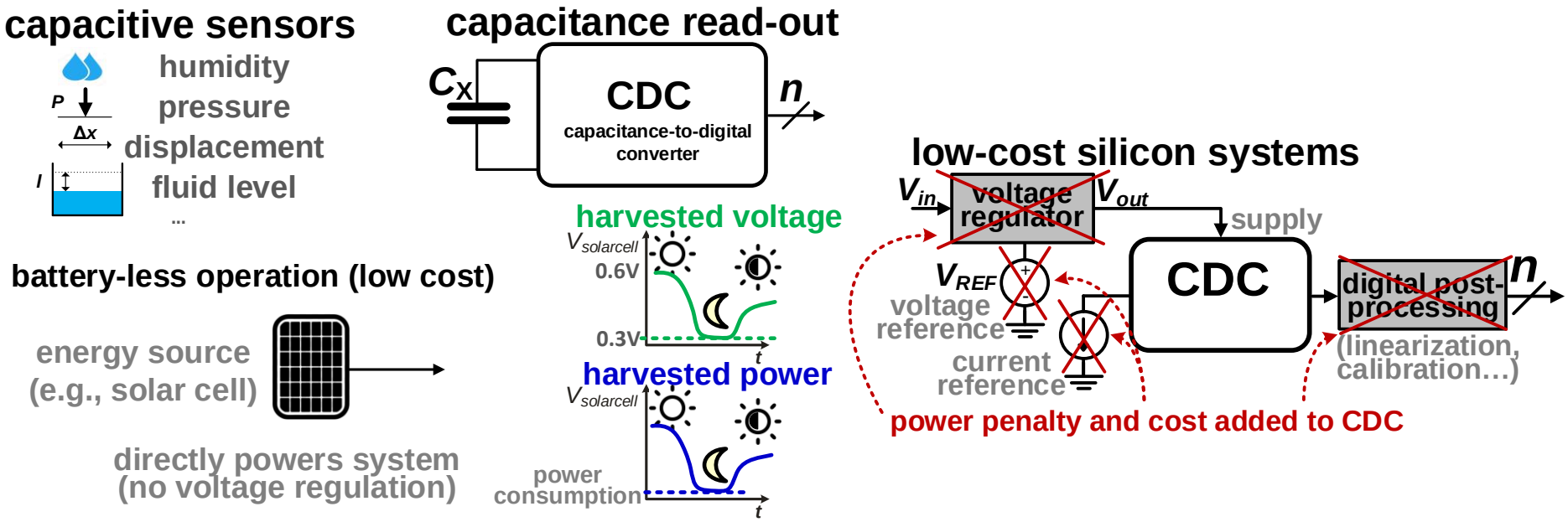
Few example of novel solutions:

- Wake-up oscillator
- DACs
- Sensor example: CDC

Conclusion

Research achievements

Capacitive-to-digital Converter (CDC)



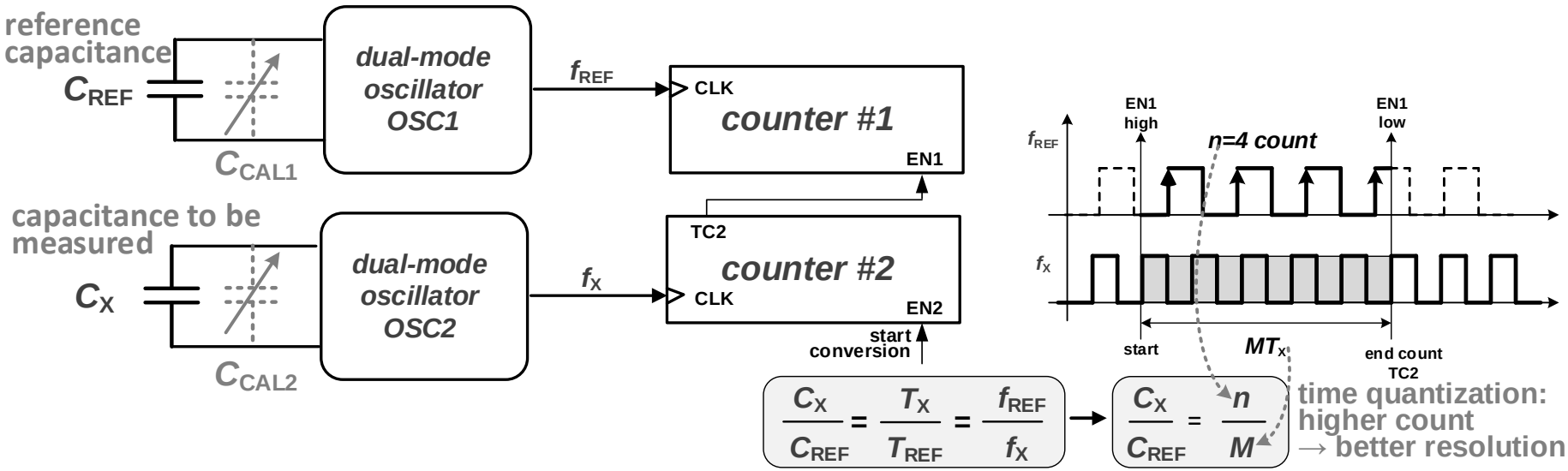
Battery-less operation: uncertain and low voltage/power

Challenge: keep power lower than harvested power, achieve low V_{min}

No Trimming, Reference and Voltage Regulation

Research achievements

CDC principle



The number of periods n of OSC1 in a pre-fixed number M of periods of OSC2 is counted, or vice-versa (swap OSC1 and OSC2)

Without mismatch, capacitance ratio = ratio of the counts

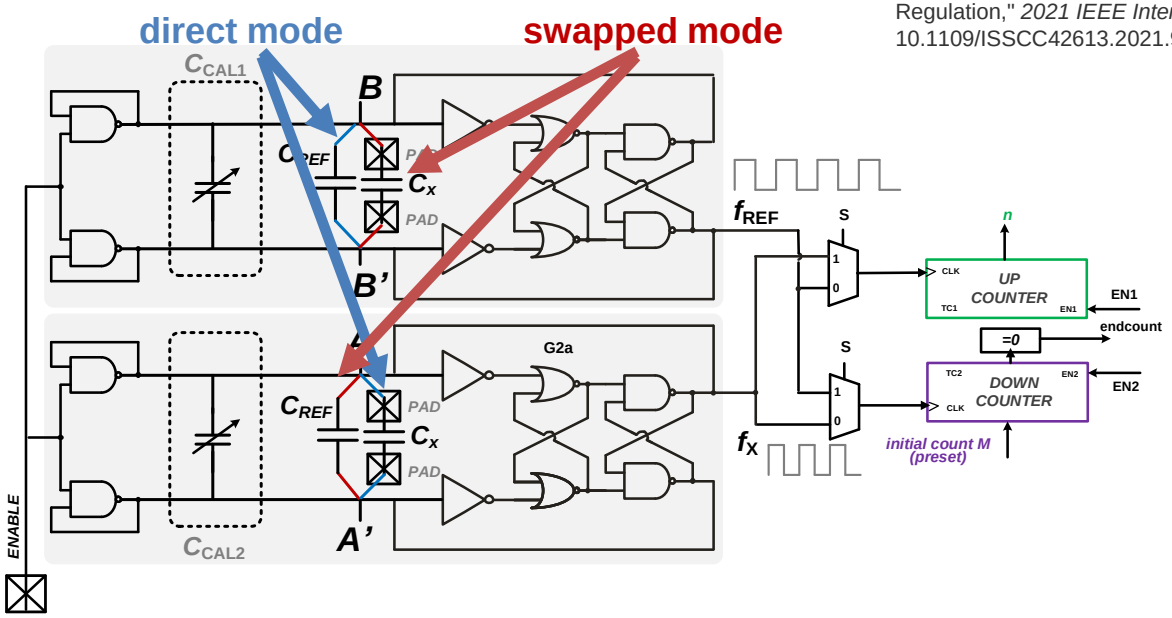
Boot-time self-calibration uses C_{CAL} to suppress mismatch

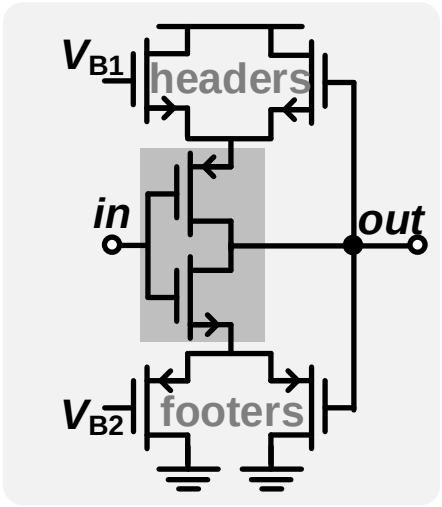
OSC1 and OSC2 track each other across global P, V and T variations

Research achievements

CDC principle

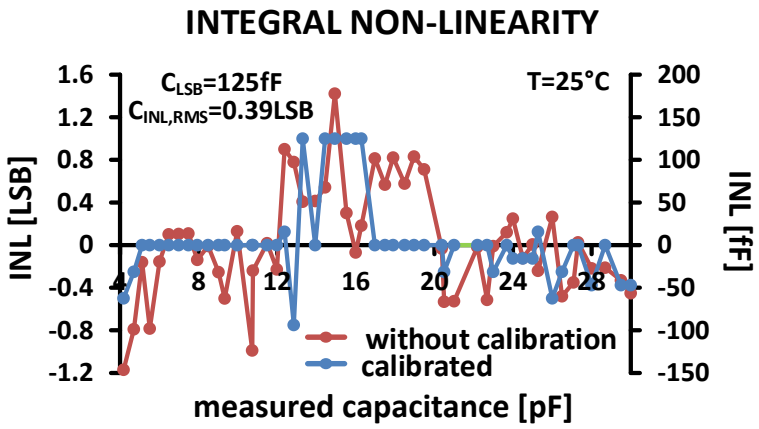
O. Aiello, P. Crovetti and M. Alioto, "5.2 Capacitance-to-Digital Converter for Operation Under Uncertain Harvested Voltage down to 0.3V with No Trimming, Reference and Voltage Regulation," *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, 2021, pp. 74-76, doi: 10.1109/ISSCC42613.2021.9365846.

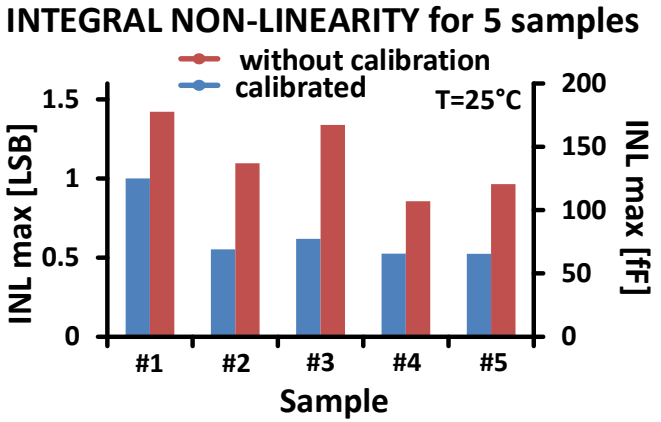


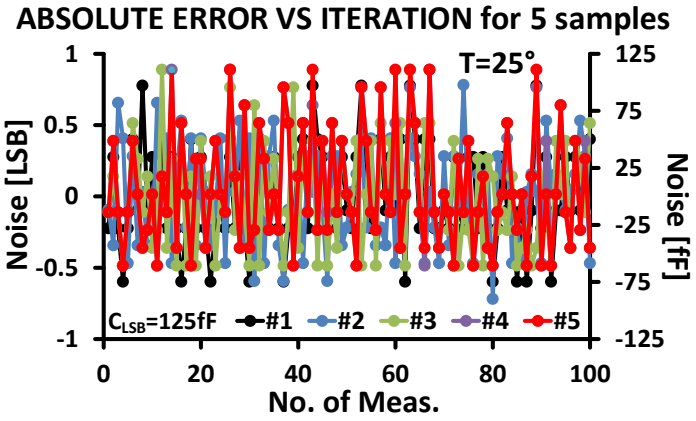


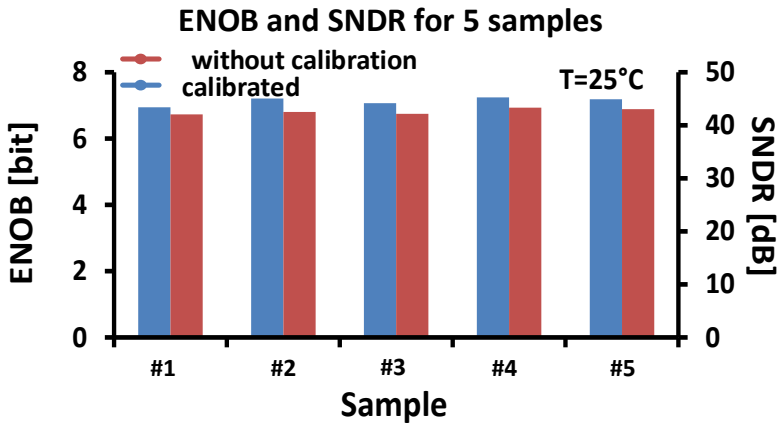
- The CDC is synthesizable and made by dual-mode logic [9] with swapped bias
- LOGIC GATE IMPLEMENTATION: swapping bias ($V_{B1} = V_{DD}$ and $V_{B2} = 0$ V) in [9]
  → ~10X lower leakage (dominant) than CMOS
- Built by Dual-Mode Logic gates → CDC robust to noise and VDD fluctuations [9]

Research achievements



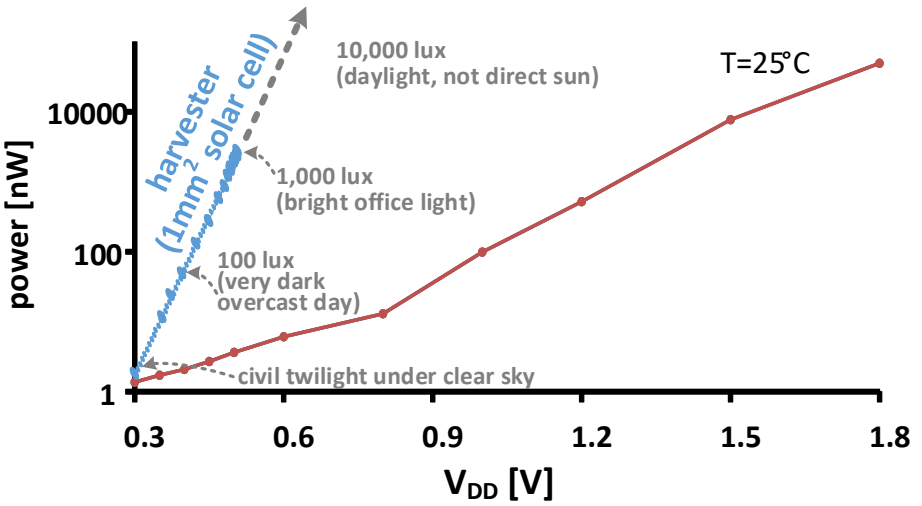


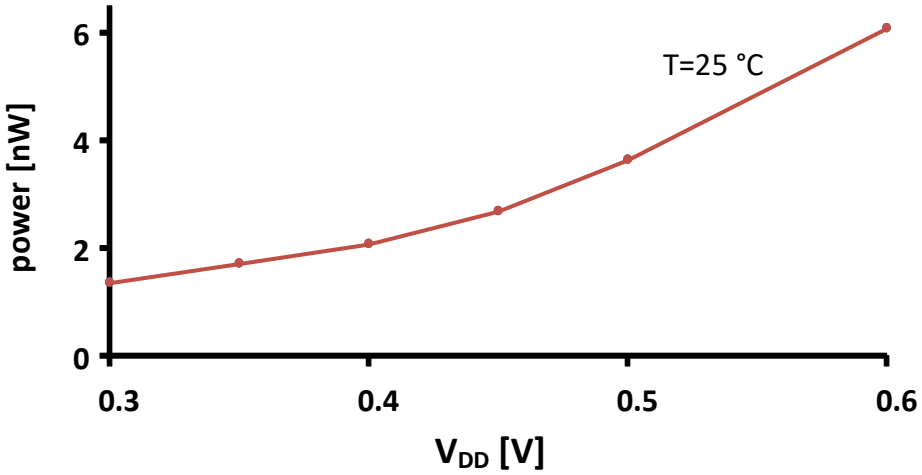




Research achievements

Power Consumption





Graceful power increase with V_{DD} (flatter than harvester) → power easily sustained at larger light intensity

Limited power increase under harvester voltage range

Outline

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Conclusion

Conclusion

Sustained by a 1-mm^2 solar cell under any practical lighting condition Lowest power consumption and widest operating power supply ever-reported in the literature for a wake-up oscillator has been fabricated.

The first fully synthesizable DACs that introduce the concept of graceful degradation have been designed and tested.

An example of fully synthesizable capacitive-to-digital converter with unregulated supply to be powered on harvesters have been also described

→ Proposed solution are highly suitable for IoT nodes.

→ Low design effort

→ Technology and Design portability among different technology nodes

→ Suitable to be powered by harvester (e.g. always-on event detection in sensor node)

Hints for your career

• Be committed.
No free-lunch (“No pain, no gain”.., but also “pain and no gain”)

• Focus on the path needed to reach your results

• Trade-off life-work balance. We are all person prior of being engineer.

• Give right importance to the right values. We are all person prior of being engineer (to be remembered)

Hints for your career

• Covid taught us the importance of social relation and face-to-face interaction: better being a "person with a name" then a number into a crowded room.

• BSc and MSc in Electronic at DITEN-UniGE give you all the mean to take-off in the job market of semiconductors: you do not need to go somewhere else ☺

• Thesis can expose you to an international scientific scenario after being fast in collecting your "near-home" exams. Better finish courses **as soon as possible and then "open yourself" in national/international mobility/experience IF you want**....

Thesis in our group are welcome :-)

Thanks for your attention

QnA

Any Questions?

Dr. Orazio Aiello
https://rubrica.unige.it/personale/UkJAUlho

My last interview on youtube:
https://www.youtube.com/watch?v=RT-VaPdJEMk

My former project