Introduction to CMOS VLSI Design

Programmable Logic

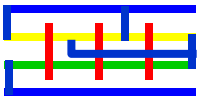
Peter Kogge Fall 2015
Includes lecture slides by David Harris, Harvey Mudd College
http://www.cmosvlsi.com/coursematerials.html

Outline

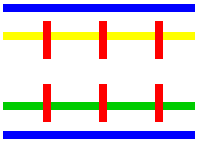
- Gate Array and Sea of Gates
- PLA
- FPGA

Sea of Gates

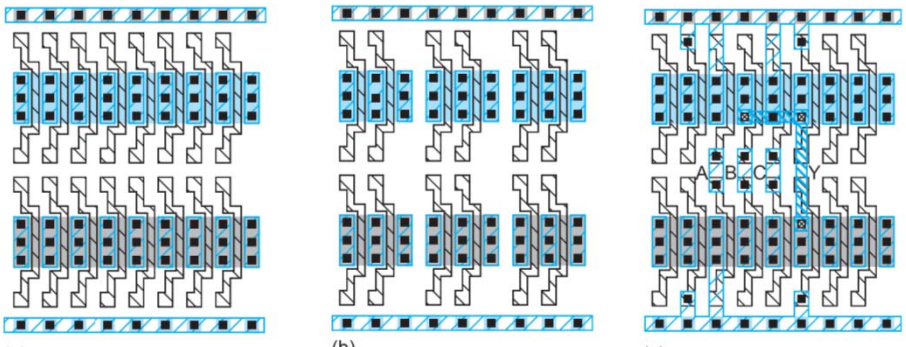
Sea of Gates



- Actually “Sea of Transistors”
- Prior standard cell design had 2 rows of diffusion
  - With taps to Gnd and Vdd to define sources
  - And metal wires to connect drains
  - And Poly going vertical
- What if we design long string of transistors on shared diffusion
  - With room for contacts to metal
- Then changing only metal masks changes logic function



Example: ~ABC



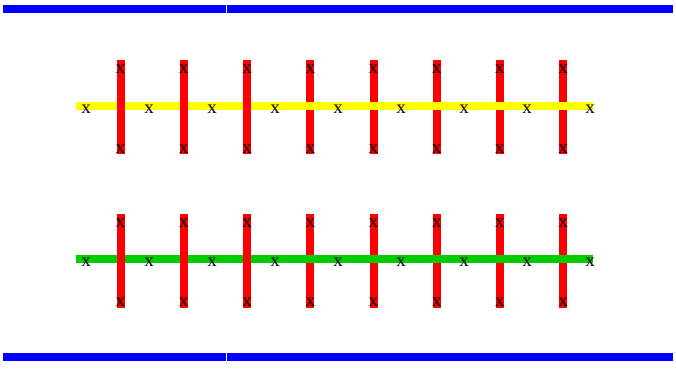
We implement a very long string

But may want multiple smaller strings

Get it by "forcing" transistors in break off.

FIGURE 14.17 SOG cell layouts

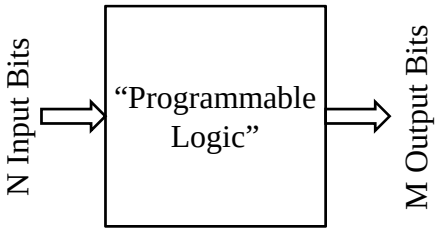
Sea of Gates as a Stick Figure



Lets do AB + CD

Programmable Logic Arrays (PLA)

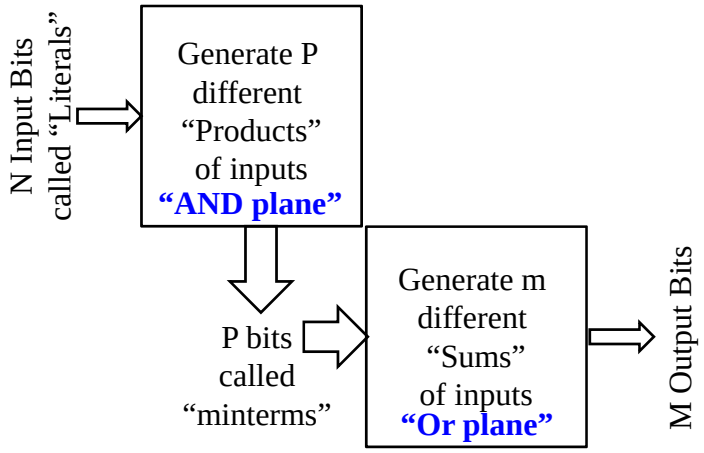
Programmable Logic



- Goal: design "Logic" once, but be able to change without total redesign
- There are $M*2^{2^N}$ different functions from N to M bits
- Two programming times
  - In final stages of design
  - Dynamically "in the field"

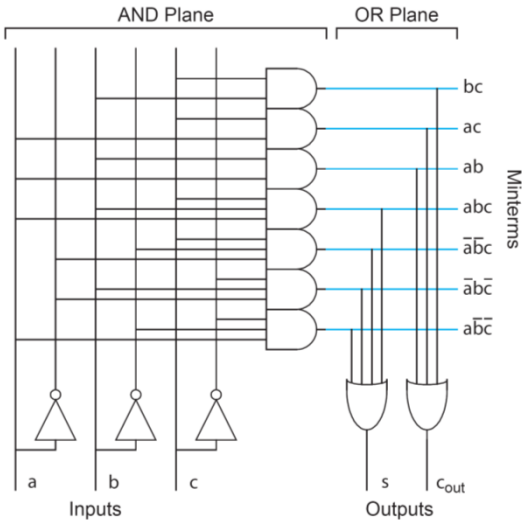
Common Approach

Express each output bit as a "sum" (OR) of "products" (AND)



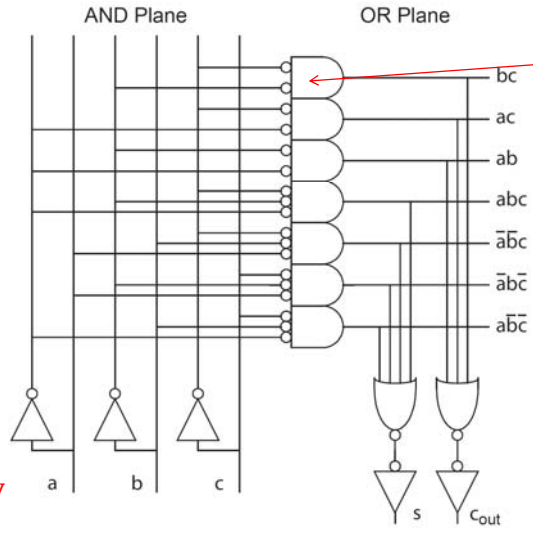
Example

- Full adder:
  - 3 input bits a, b, c
  - 2 output bits s, cout
- s = abc + ~a~bc + ~ab~c + a~b~c
- cout = abc + ab + ac + bc
- There are 7 product terms
  - abc, ~a~bc, ~ab~c, a~b~c, ab, ac, bc
- Each output is OR of 4 of these
  - One term is reused twice



If we invert the inputs to the ANDs we can replace by NORs

FIGURE 12.73 OR/NOR representation of PLA



Equivalent to a NOR

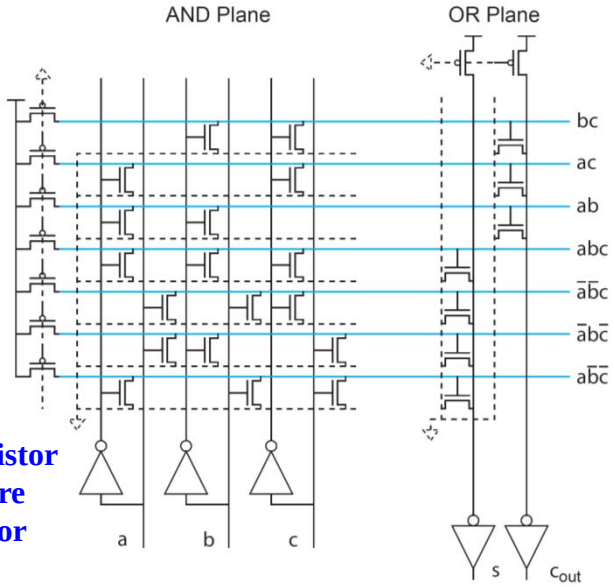
Question: why choose NORs

FIGURE 12.75 AND/OR representation of PLA

PLAs with NOR Gates

- AND plane: P NOR gates
  - Each with **2N** "possible" inputs
    - input[k] and not(input[k])
  - Programming: specify which subset of possible inputs to use for each product
- OR plane: M NOR gates
  - Each with inverter on output
  - Each with P "possible" inputs
  - Programming: specify which subset of possible minterms to use for each sum

FIGURE 12.74 Dot diagram representation of PLA



Place a transistor wherever there is a "•" in prior figure

FIGURE 12.76 Pseudo-nMOS PLA schematic

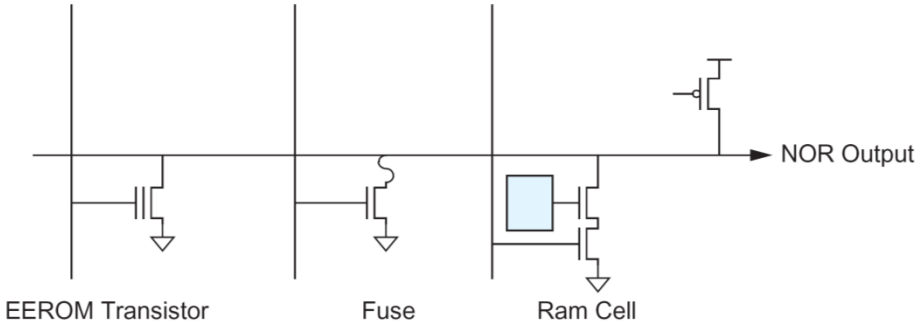


FIGURE 14.14 PLA NOR structure (one plane shown)

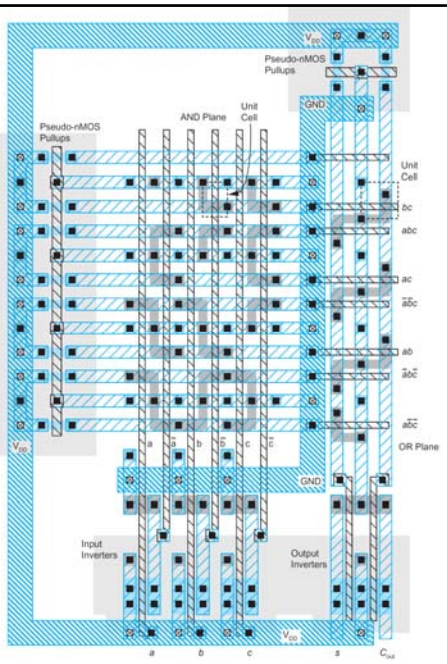


FIGURE 12.77 Pseudo-nMOS PLA layout

Field Programmable Logic Array

FPGAs

- ***AT ANY TIME*** load a string of bits into device
- Bits do several things
  - Configure each of many **Configurable Logic Blocks (CLB)** to perform some specific logic function
  - Configure which outputs of which CLBs are connected to inputs of which other CLBs
  - Configure which pins on device are connected to which CLB

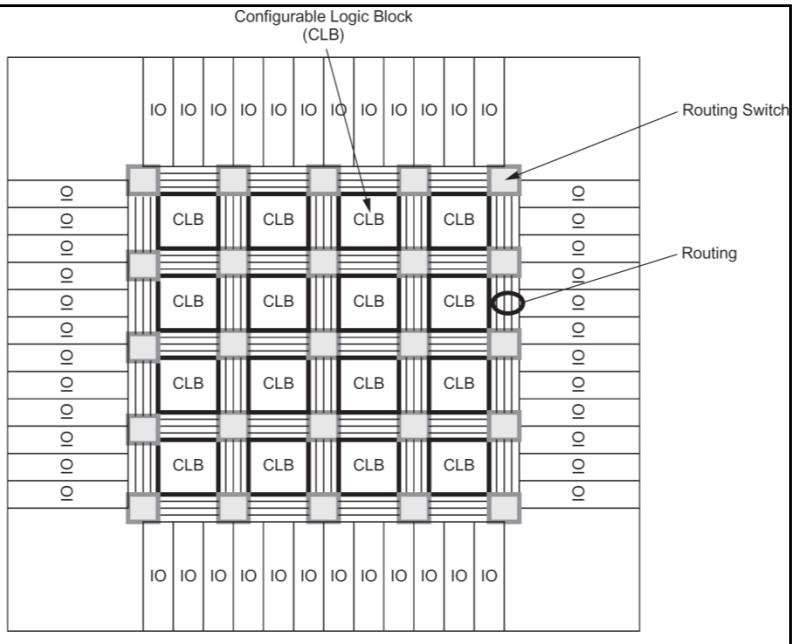
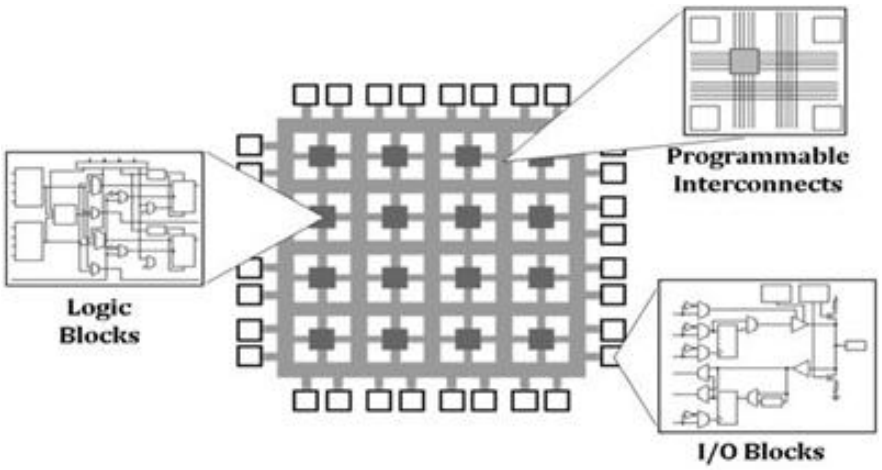


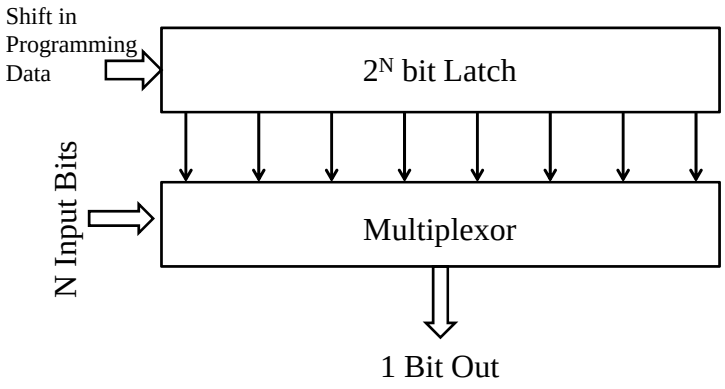
FIGURE 14.15 Simplified FPGA floorplan

A Bit More...



http://www.ni.com/cms/images/devzone/tut/figure3-%20fpga_400x212.jpg

Look Up Table (LUT)



To Get M outputs, Use M LUTs

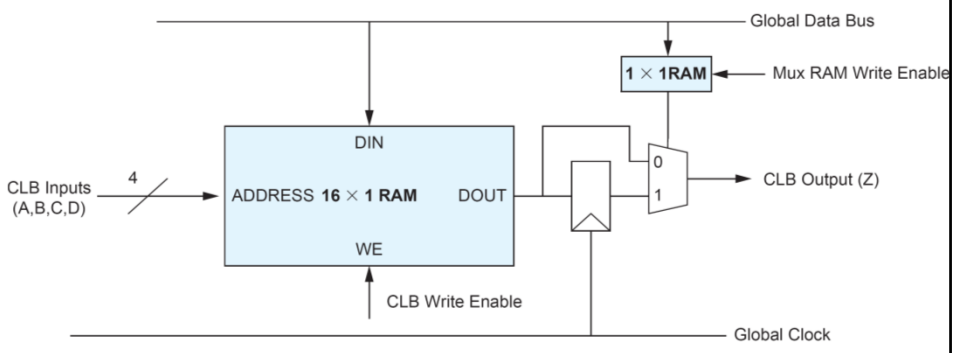
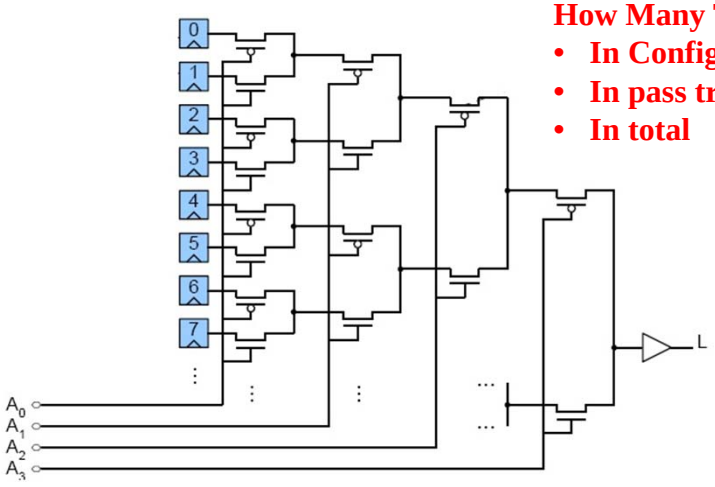


FIGURE 14.16 Simple FPGA logic cell

If we used a 16 bit SRAM, that's 6*16+row decoders, sense amps…
Can we do better?

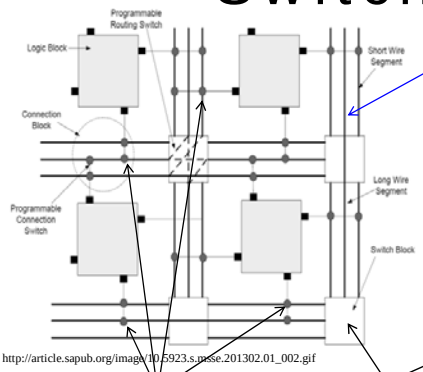
Alternative 4-Input LUT



How Many Transistors?

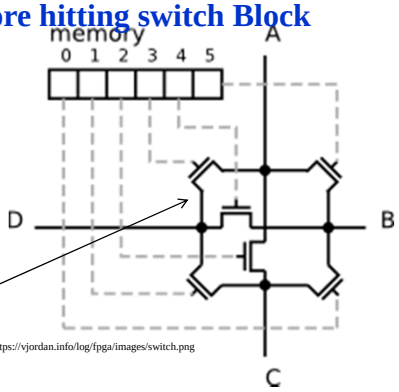
- **In Config Reg**
- **In pass tree**
- **In total**

Switch Matrix



http://article.sapub.org/image/10.5923.s.msse.201302.01_002.gif

"Long Wires" go further before hitting switch Block



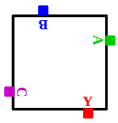
https://vjordan.info/log/fpga/images/switch.png

Each ● here is one of these

Each switch block is array of Switches

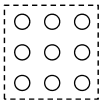
Six configuration bits allow complete freedom in connecting A, B, C, D, with signals that can go in either direction.

Notation for Next Slide



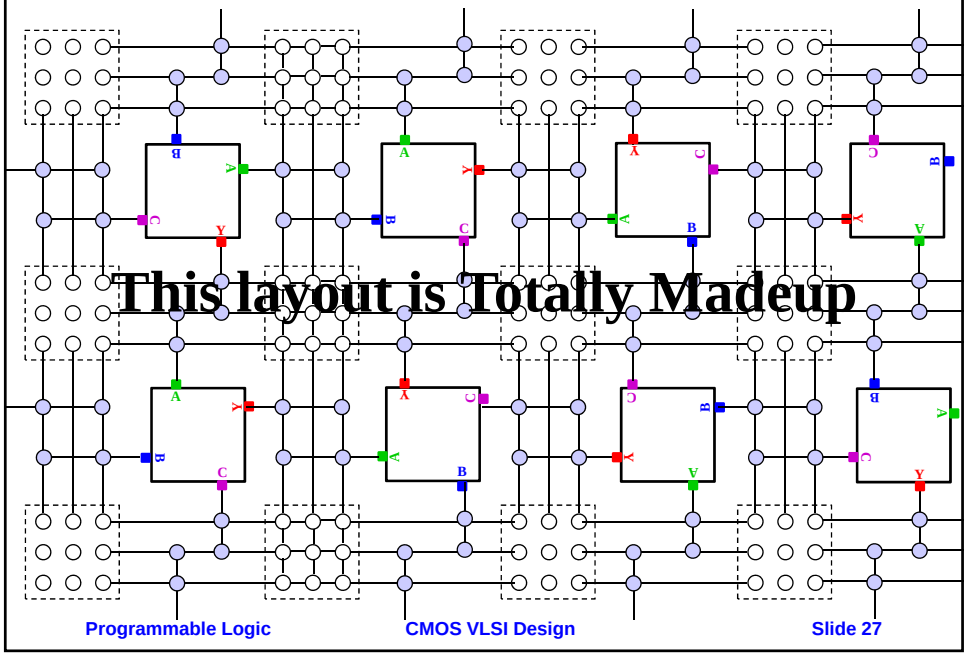
3-Input LUT with inputs A, B, C ant Output Y

If "X"ed, then horizontal and vertical wires connected
If not, horizontal and vertical wires are separate

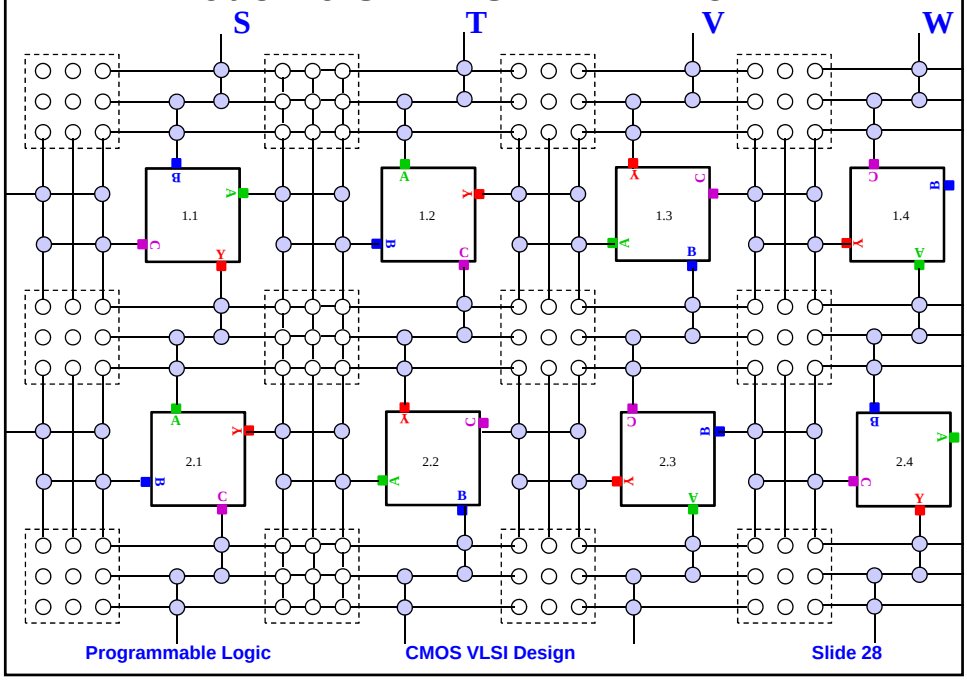


Switch Box: Each circle can be programmed for any of the 64 possible thru connections

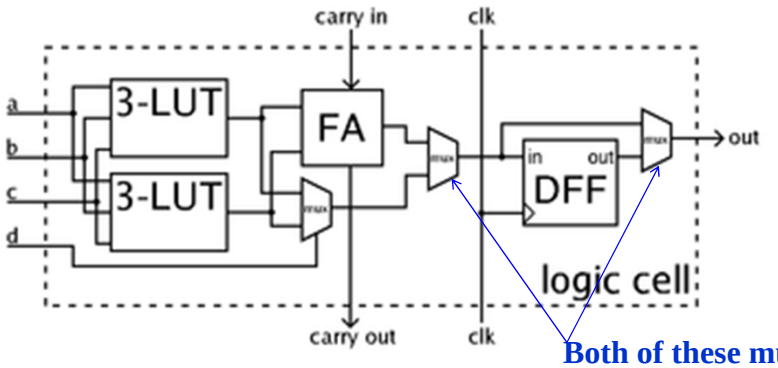
Sea of 3-Input LUTs



Let's Do ST + ~SVW + ~T~U~W



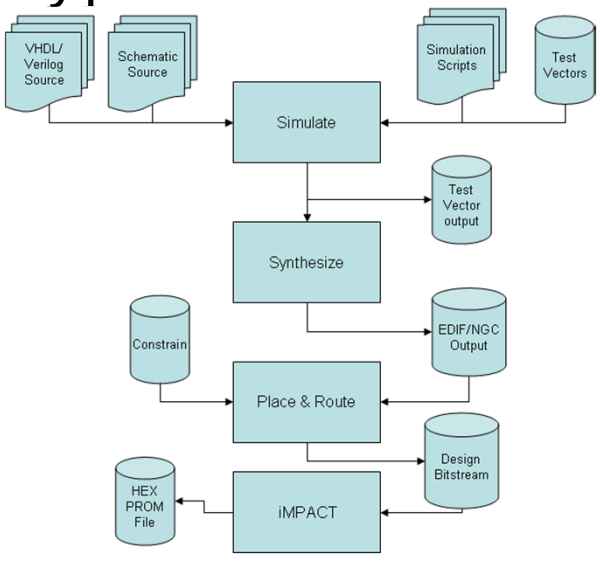
A More Typical 4-input 1 Output CLB



https://en.wikipedia.org/wiki/File:FPGA_cell_example.png

Both of these muxes are driven by other configuration bits

Typical Tool Chain



http://www.codeproject.com/KB/system/fpgaflow/01_fpgaflow_s.png

A Recent Product Table

Arria 10 Product Table

	Product Line	GX 160 SX 160	GX 220 SX 220	GX 270 SX 270	GX 320 SX 320	GX 480 SX 480	GX 570 SX 570	GX 660 SX 660	GX 900	GX 1150	GT 900	GT 1150
Resources	Part number reference	10AX016 / 10AS016	10AX022 / 10AS022	10AX027 / 10AS027	10AX032 / 10AS032	10AX048 / 10AS048	10AX057 / 10AS057	10AX066 / 10AS066	10AX090	10AX115	10AT090	10AT115
	Logic elements (K)	160	220	270	320	480	570	660	900	1,150	900	1,150
	Adaptive logic modules (ALMs)	61,510	83,730	101,620	118,730	181,790	217,080	250,540	339,620	427,200	339,620	427,200
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160	1,358,480	1,708,800	1,358,480	1,708,800
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133	2,423	2,713	2,423	2,713
	M20K memory (Mb)	9	11	15	17	28	35	42	47	53	47	53
	MLAB memory (Mb)	1.0	1.8	2.4	2.8	4.3	5.0	5.7	9.2	12.7	9.2	12.7
	Hardened single-precision floating-point multipliers/adders	156/156	191/191	830/830	985/985	1,368/1,368	1,523/1,523	1,688/1,688	1,518/1,518	1,518/1,518	1,518/1,518	1,518/1,518
	18 x 19 multipliers	312	382	1,660	1,970	2,736	3,046	3,376	3,036	3,036	3,036	3,036
	Peak GMACS	343	420	1,826	2,167	3,010	3,351	3,714	3,340	3,340	3,340	3,340
	Peak giga floating-point operation per second (GFLOPS)	140	172	747	887	1,231	1,371	1,519	1,366	1,366	1,366	1,366
Clocks and Maximum I/O Pins	Regional clocks	8	8	8	8	8	8	16	16	16	16	16
	Maximum LVDS channels (1.6 G)	120	120	168	168	222	270	270	384	384	312	312
	Maximum user I/O pins	288	288	384	384	492	624	624	768	768	624	624
	Transceiver count (17.4 Gbps)	12	12	24	24	36	48	48	96	96	96	96
	Transceiver count (28 Gbps)	–	–	–	–	–	–	–	–	–	16	16
	PCI Express® (PCIe®) hard IP blocks (Gen3)	1	1	2	2	2	2	2	4	4	4	4
	Maximum 3 V I/O pins	48	48	48	48	48	48	48	–	–	–	–

https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/pt/arria-10-product-table.pdf

Worksheets