UNIT II

CIRCUIT DESIGN PROCESSES

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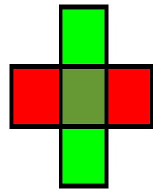
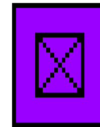
INTRODUCTION

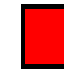
- Objectives:
  - To know MOS layers
  - To understand the stick diagrams
  - To learn design rules
  - To understand layout and symbolic diagrams

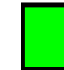
- Outcome:
  - At the end of this, will be able draw the stick diagram, layout and symbolic diagram for simple MOS circuits

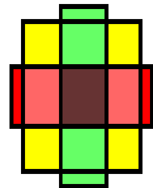
MOS LAYERS

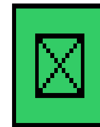

Transistor

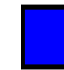

Metal-Polysilicon

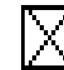

Polysilicon

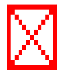

Diffusion

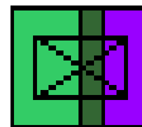

Depletion Transistor


Metal-Diffusion


Metal


Contact


Polysilicon Pin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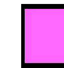
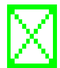
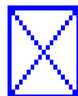
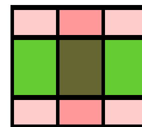
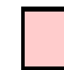

Implant


Diffusion Pin

Overglass


Metal Pin


Buried


Buried

STICK DIAGRAMS

- Objectives:
  - To know what is meant by stick diagram.
  - To understand the capabilities and limitations of stick diagram.
  - To learn how to draw stick diagrams for a given MOS circuit.

- Outcome:
  - At the end of this module the students will be able draw the stick diagram for simple MOS circuits.

STICK DIAGRAMS

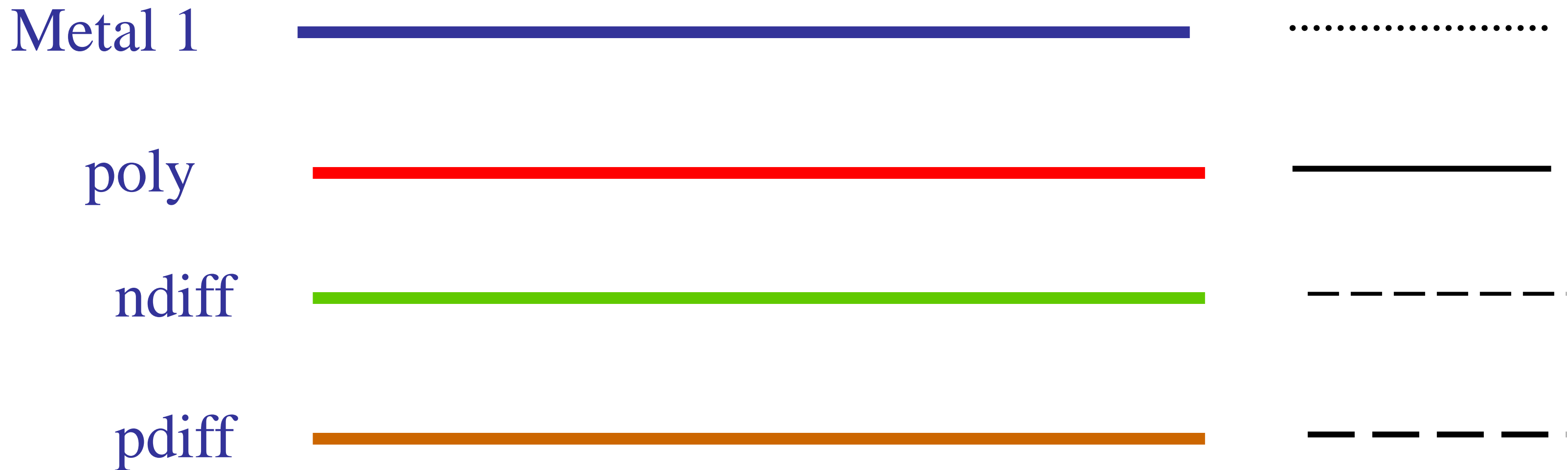
- VLSI design aims to translate circuit concepts onto silicon.
- Stick diagrams are a means of capturing topography and layer information using simple diagrams.
- Stick diagrams convey layer information through color codes (or monochrome encoding).
- Acts as an interface between symbolic circuit and the actual layout.

- Does show all components/vias.
  - Via is used to connect higher level metals from metal connection
- It shows relative placement of components.
- Goes one step closer to the layout
- Helps plan the layout and routing

A stick diagram is a cartoon of a layout.

- Does ***not*** show
  - Exact placement of components
  - Transistor sizes
  - Wire lengths, wire widths, tub boundaries
  - Any other low level details such as parasitics

Stick Diagrams – Notations



Buried Contact

Contact Cut

STICK DIAGRAMS

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN		n-diffusion (n+ active) Thinox*	*Thinox = n-diff. + transistor channels	ND
RED		Polysilicon		NP
BLUE		Metal 1		NM
BLACK		Contact cut		NC
GRAY	NOT APPLICABLE	Overglass		NG
nMOS ONLY YELLOW		Implant		NI
nMOS ONLY BROWN		Buried contact		NB

FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor	D, S, L: W, G; S, D, L: W, G	L: W, S, G, D	(L: W = 1:1), S, D, G
Transistor length to width ratio L: W should be shown.			
n-type depletion mode transistor nMOS only	L: W; L: W	L: W, S, G, D	(L: W = 1:1)
	Source, drain and gate labelling will not normally be shown.		

NMOS ENCODING

STICK DIAGRAMS

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN	Encoding as in Color plate 1(a)	n-diffusion (n+ active) Thinox*	* Thinox = n-diff. + p-diff. + transistor channels Encoding as in Color plate 1(a)	CAA or CNA
RED		Polysilicon		CPG
BLUE		Metal 1		CMF
BLACK		Contact cut		CC
GRAY		Overglass		COG
YELLOW (STICK)	green outline here for clarity	p-diffusion (p+ active)	p+ mask	CAA or CPA
YELLOW	Not shown on diagram	p+ mask	either or	CPP
DARK BLUE OR PURPLE		Metal 2		CMS
BLACK		VIA		CVA
BROWN	Demarcation line p-well edge is shown as a demarcation line in stick diagrams	p-well		CPW
BLACK	X	V_{DD} or V_{SS} contact	V_{DD} V_{SS}	CC

FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor (as in Color plate 1(a))	Demarcation line L:W		
Transistor length to width ratio L:W may be shown.			
p-type enhancement mode transistor	L:W S G D Demarcation line	S G D	S D G p+ mask

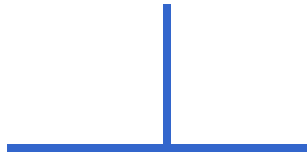
Note: p-type transistors are placed above and n-type below the demarcation line

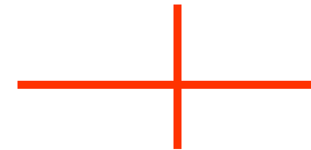
CMOS ENCODING

Stick Diagrams – Some Rules

Rule 1:

When two or more 'sticks' of the same type cross or touch each other that represents electrical contact.





Stick Diagrams – Some Rules

Rule 2:

When two or more ‘sticks’ of different type cross or touch each other there is no electrical contact.

(If electrical contact is needed we have to show the connection explicitly)

Stick Diagrams – Some Rules

Rule 3:

When a poly crosses diffusion it represents a transistor.

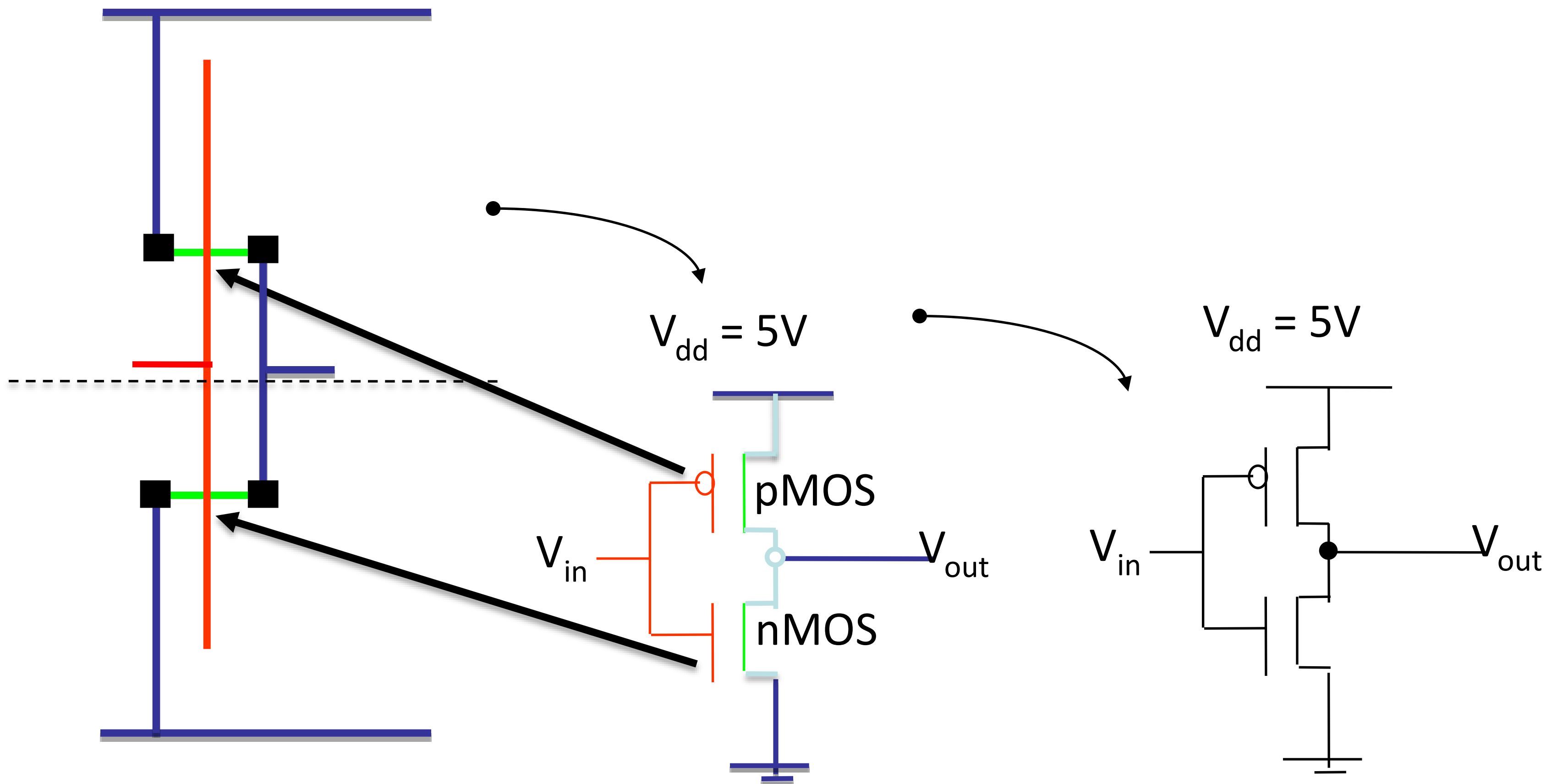
Note: If a contact is shown then it is ***not*** a transistor.

Stick Diagrams – Some Rules

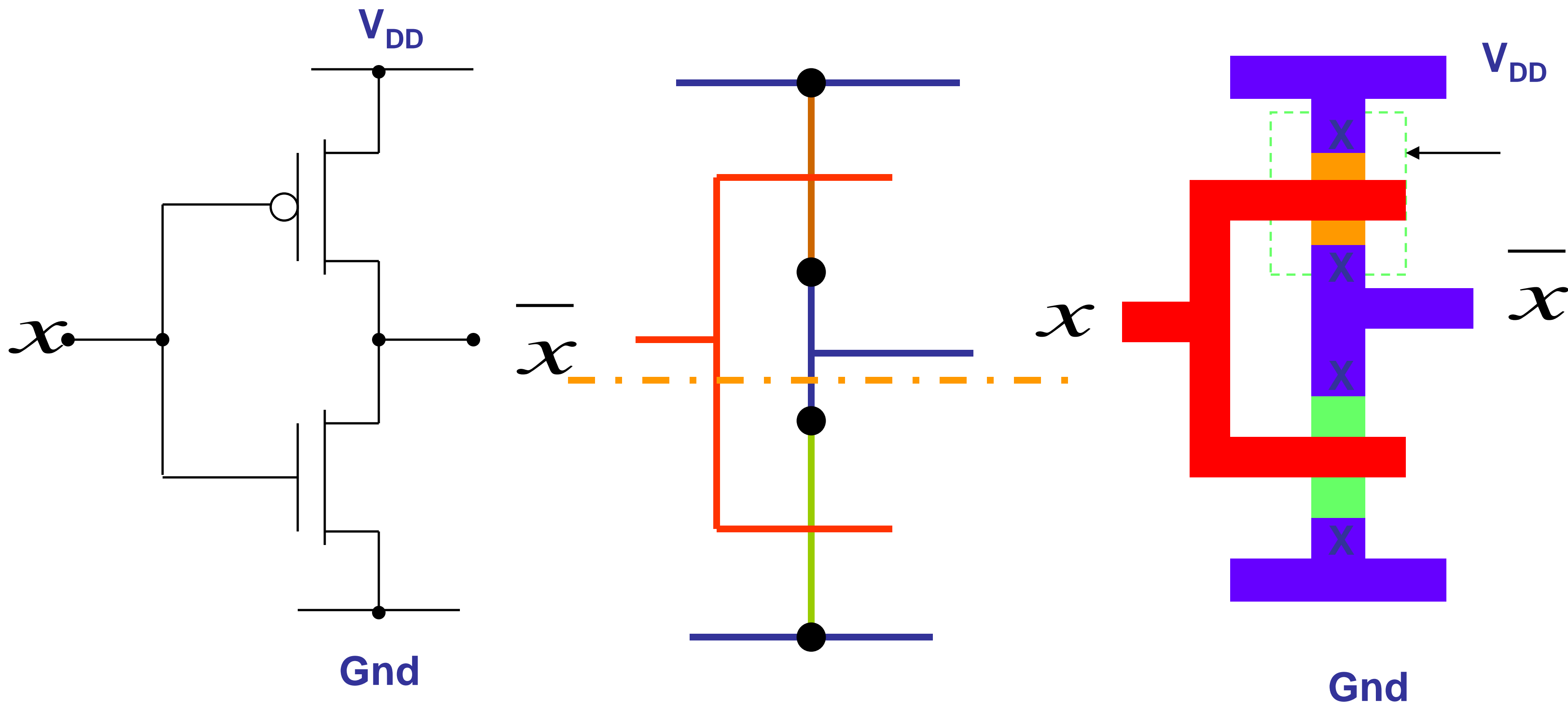
Rule 4:

In CMOS a demarcation line is drawn to avoid touching of p-diff with n-diff. All PMOS must lie on one side of the line and all NMOS will have to be on the other side.

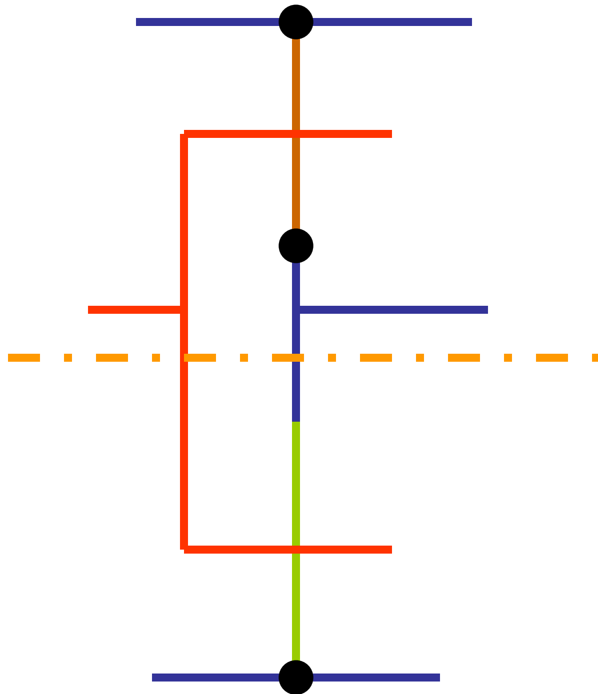
Examples of Stick Diagrams

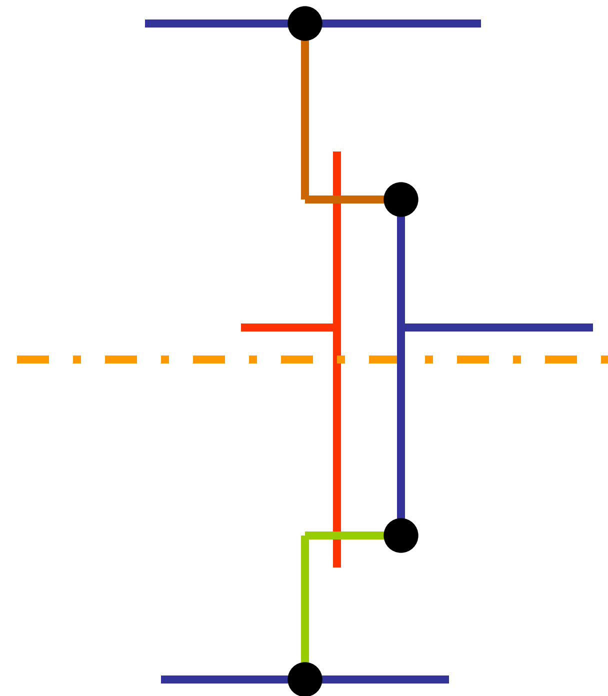


Examples of Stick Diagrams

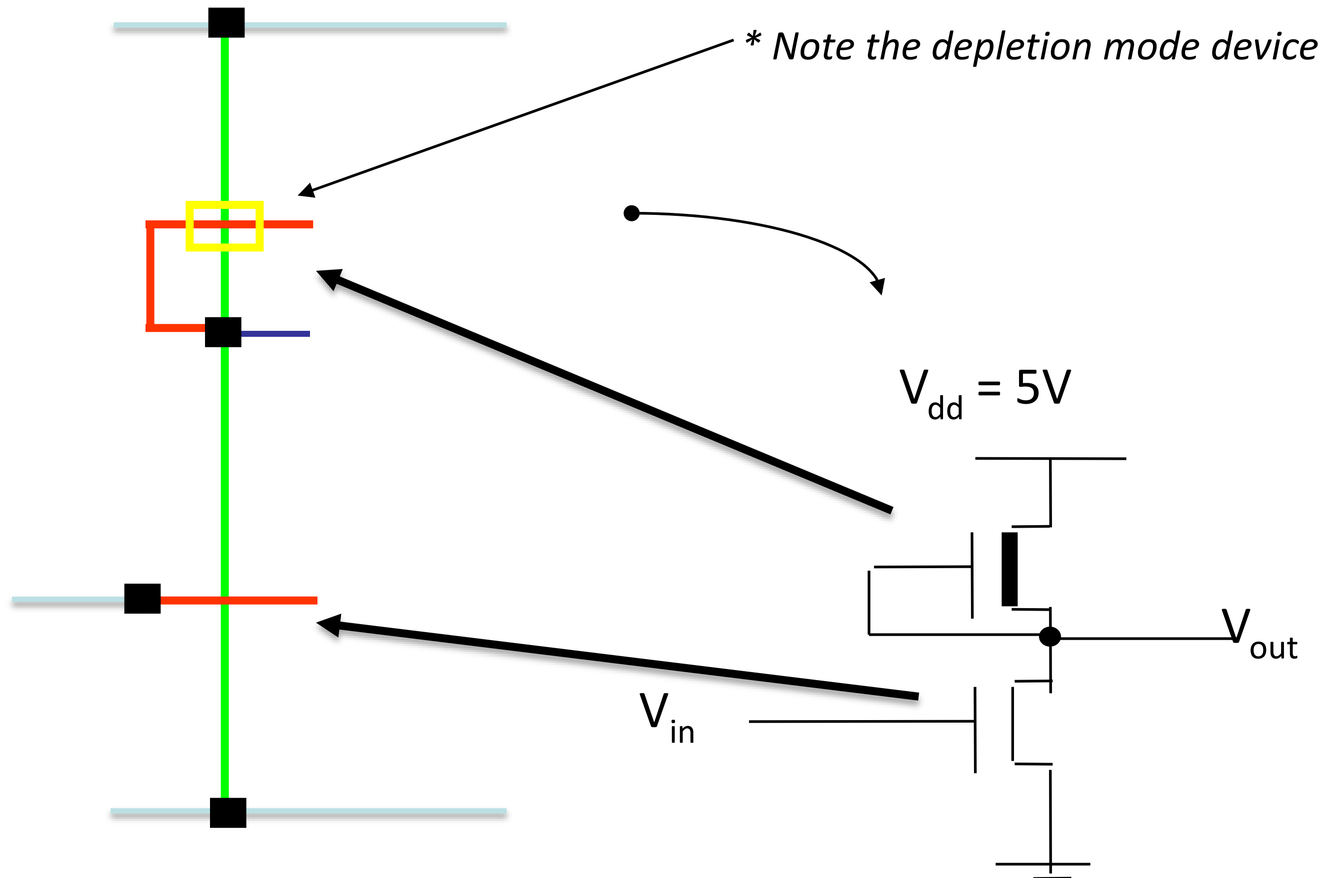


Examples of Stick Diagrams

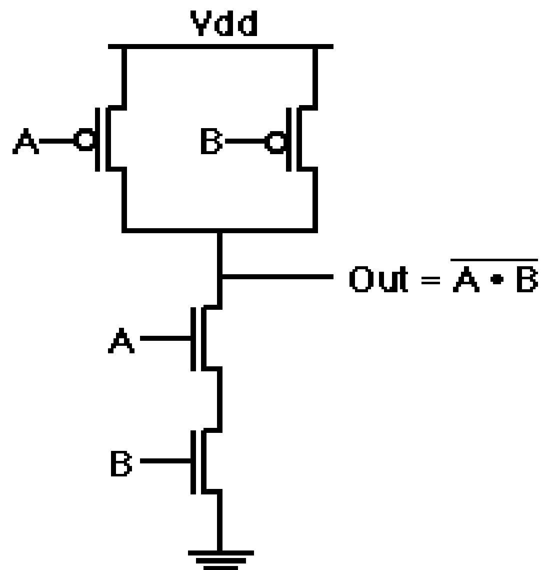




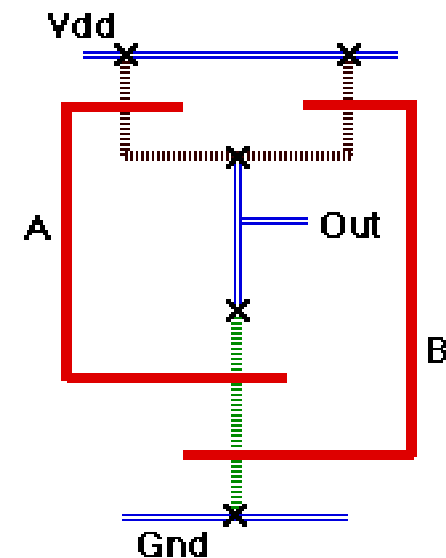
Examples of Stick Diagrams



Examples of Stick Diagrams

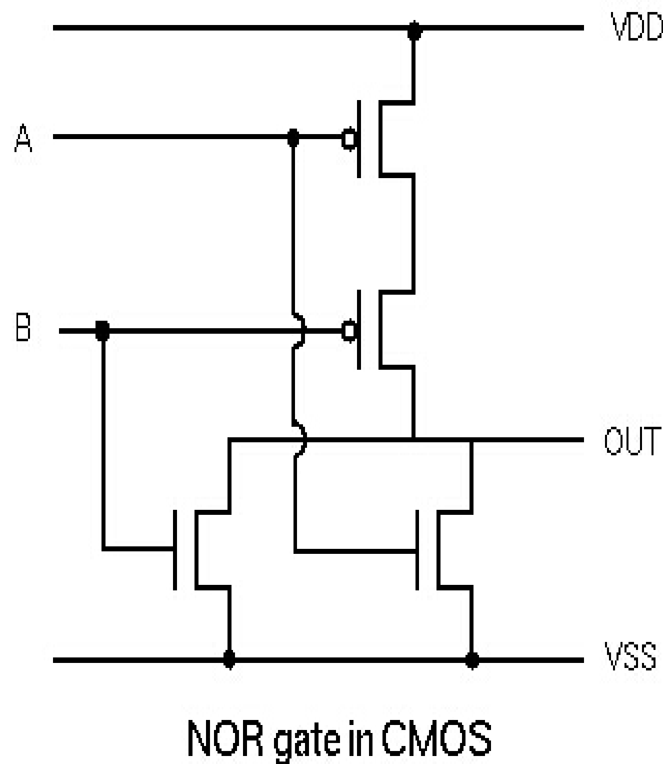


A	B	$\overline{A \bullet B}$
0	0	1
0	1	1
1	0	1
1	1	0

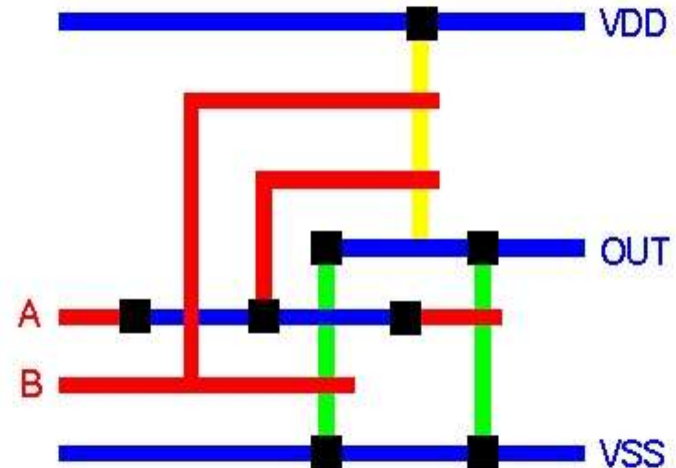


1. Pull-down: Connect to ground If A=1 AND B=1
2. Pull-up: Connect to Vdd If A=0 OR B=0

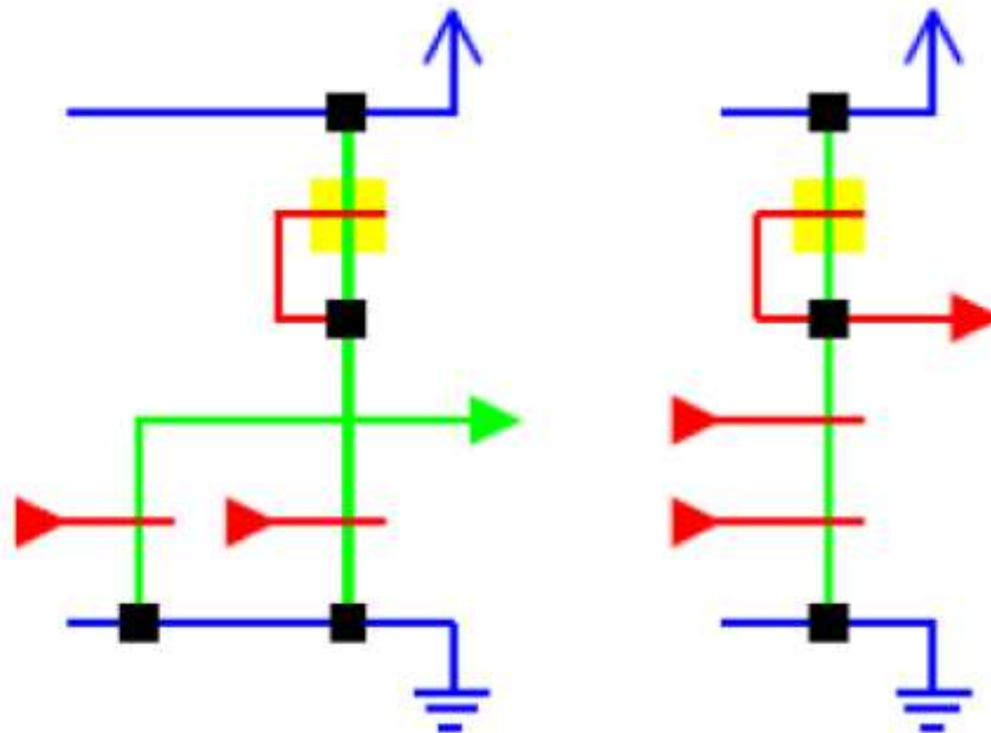
Examples of Stick Diagrams



NOR gate in CMOS

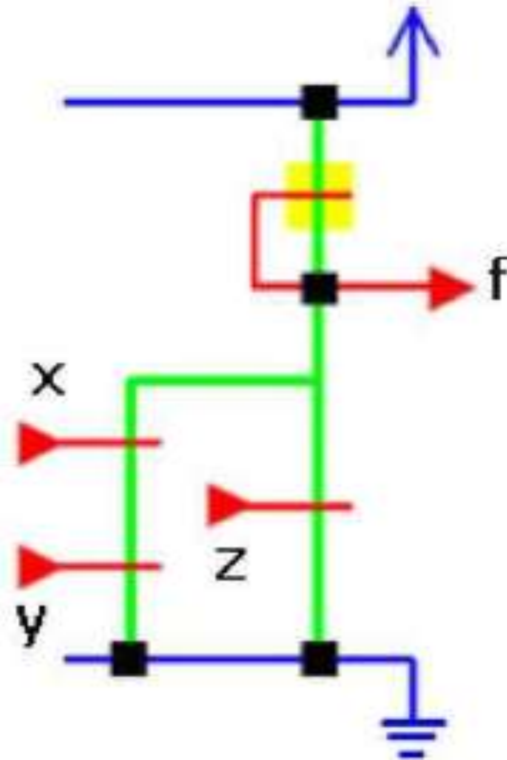


Examples of Stick Diagrams



NOR gate and NAND using NMOS Transistors

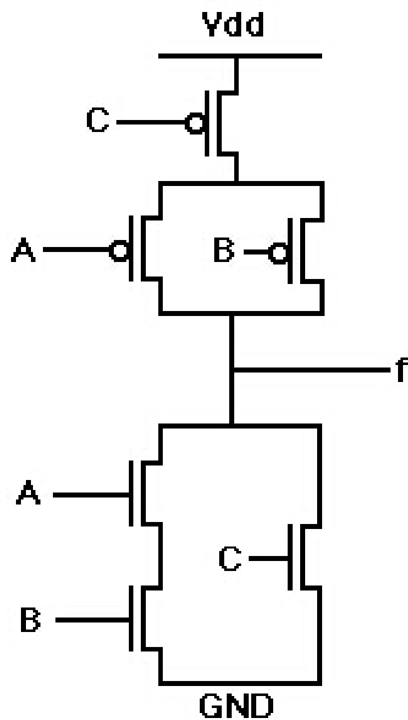
Examples of Stick Diagrams

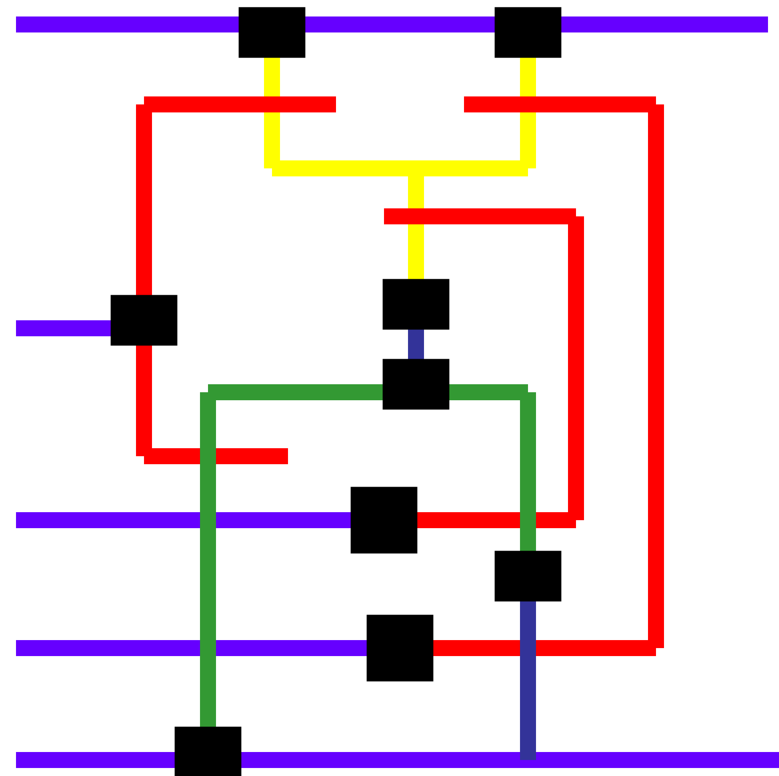


f= [(xy) +z]’ using NMOS Transistors

Examples of Stick Diagrams

Example: $f = \overline{(A \bullet B) + C}$





DESIGN RULES

- **Why we use design rules?**
  - Interface between designer and process engineer

- Historically, the process technology referred to the length of the silicon channel between the source and drain terminals in field effect transistors.
- The sizes of other features are generally derived as a ratio of the channel length, where some may be larger than the channel size and some smaller.
  - For example, in a 90 nm process, the length of the channel may be 90 nm, but the width of the gate terminal may be only 50 nm.

DESIGN RULES

Semiconductor manufacturing processes
- 10 µm — 1971 - 3 µm — 1975 - 1.5 µm — 1982 - 1 µm — 1985 - 800 nm (0.80 µm) — 1989 - 600 nm (0.60 µm) — 1994 - 350 nm (0.35 µm) — 1995 - 250 nm (0.25 µm) — 1998 - **180 nm** (0.18 µm) — 1999 - 130 nm (0.13 µm) — 2000 - 90 nm — 2002 - 65 nm — 2006 - 45 nm — 2008 - 32 nm — 2010 - 22 nm — approx. 2011 - 16 nm — approx. 2018 - 11 nm — approx. 2022

DESIGN RULES

- Allow translation of circuits (usually in stick diagram or symbolic form) into actual geometry in silicon
- Interface between circuit designer and fabrication engineer
- Compromise
  - designer - tighter, smaller
  - fabricator - controllable, reproducible

DESIGN RULES

- Design rules define ranges for features
  - Examples:
    - min. wire widths to avoid breaks
    - min. spacing to avoid shorts
    - minimum overlaps to ensure complete overlaps
  - Measured in microns
  - Required for resolution/tolerances of masks
- Fabrication processes defined by minimum channel width
  - Also minimum width of poly traces
  - Defines "how fast" a fabrication process is

DESIGN RULES

- **Two major approaches:**
  - **"Micron" rules: stated at micron resolution.**
  - **λ rules: simplified micron rules with limited scaling attributes.**
- **Design rules represents a tolerance which insures very high probability of correct fabrication**
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

“Micron” rules

- All minimum sizes and spacing specified in microns.
- Rules don't have to be multiples of λ.
- Can result in 50% reduction in area over λ based rules
- Standard in industry.

Lambda-based Design Rules

- *Lambda-based* (scalable CMOS) design rules define scalable rules based on λ (which is half of the minimum channel length)
  - classes of MOSIS SCMOS rules: SUBMICRON, DEEPSUBMICRON
- Stick diagram is a draft of real layout, it serves as an abstract view between the schematic and layout.

Lambda-based Design Rules

- Circuit designer in general want tighter, smaller layouts for improved performance and decreased silicon area.
- On the other hand, the process engineer wants design rules that result in a controllable and reproducible process.
- Generally we find there has to be a compromise for a competitive circuit to be produced at a reasonable cost.
- All widths, spacing, and distances are written in the form
- $\lambda = 0.5$ X minimum drawn transistor length

Lambda-based Design Rules

- Design rules based on single parameter, λ
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- If design rules are obeyed, masks will produce working circuits
- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

Design Rules – Reality

- Manufacturing processes have inherent limitations in accuracy and repeatability
- Design rules specify geometry of masks that provide reasonable yield
- Design rules are determined by experience

Problems in Manufacturing

- Photoresist shrinking / tearing
- Variations in material deposition
- Variations in temperature
- Variations in oxide thickness
- Impurities
- Variations between lots
- Variations across the wafer

Problems in Manufacturing

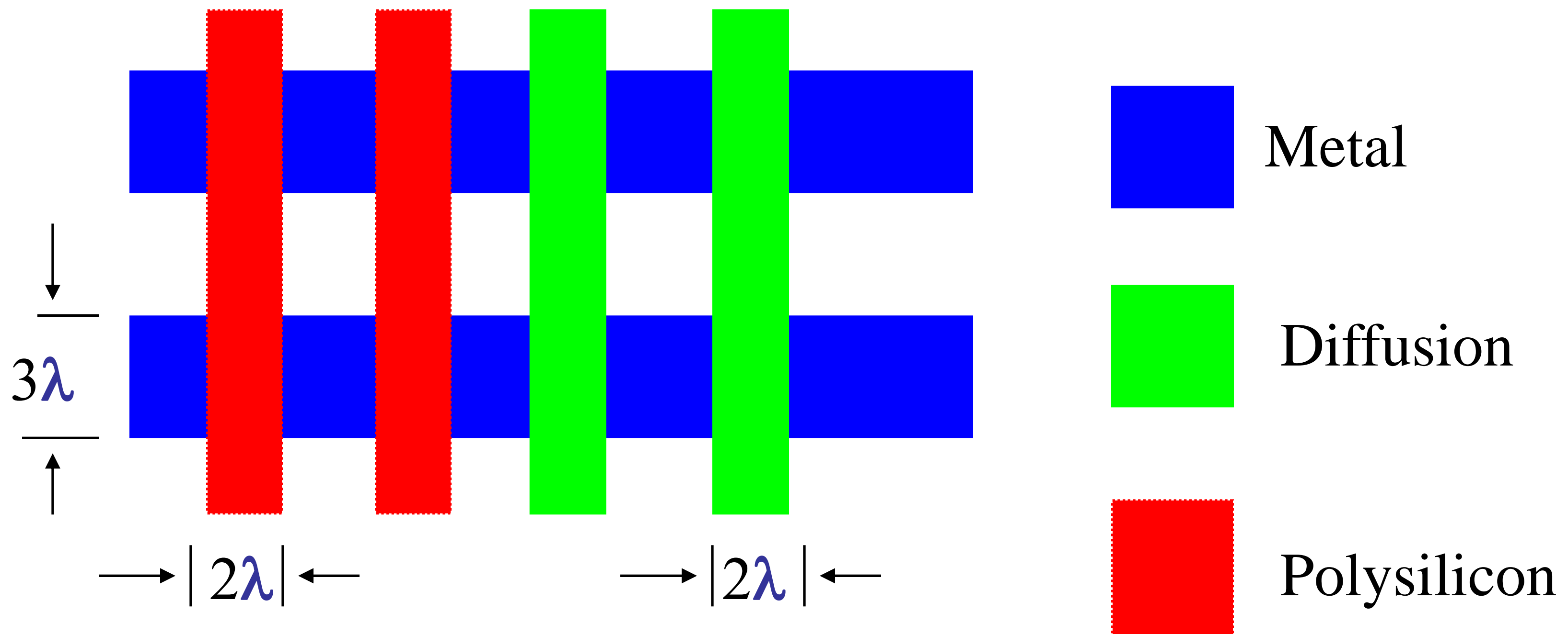
- Variations in threshold voltage
  - oxide thickness
  - ion implantation
  - poly variations
- Diffusion - changes in doping (variation in R, C)
- Poly, metal variations in height and width
- Shorts and opens
- Via may not be cut all the way through
- Undersize via has too much resistance
- Oversize via may short

Advantages of Generalized Design Rules

- Ease of learning because they are scalable, portable, durable
- Long-levity of designs that are simple, abstract and minimal clutter
- Increased designer efficiency
- Automatic translation to final layout

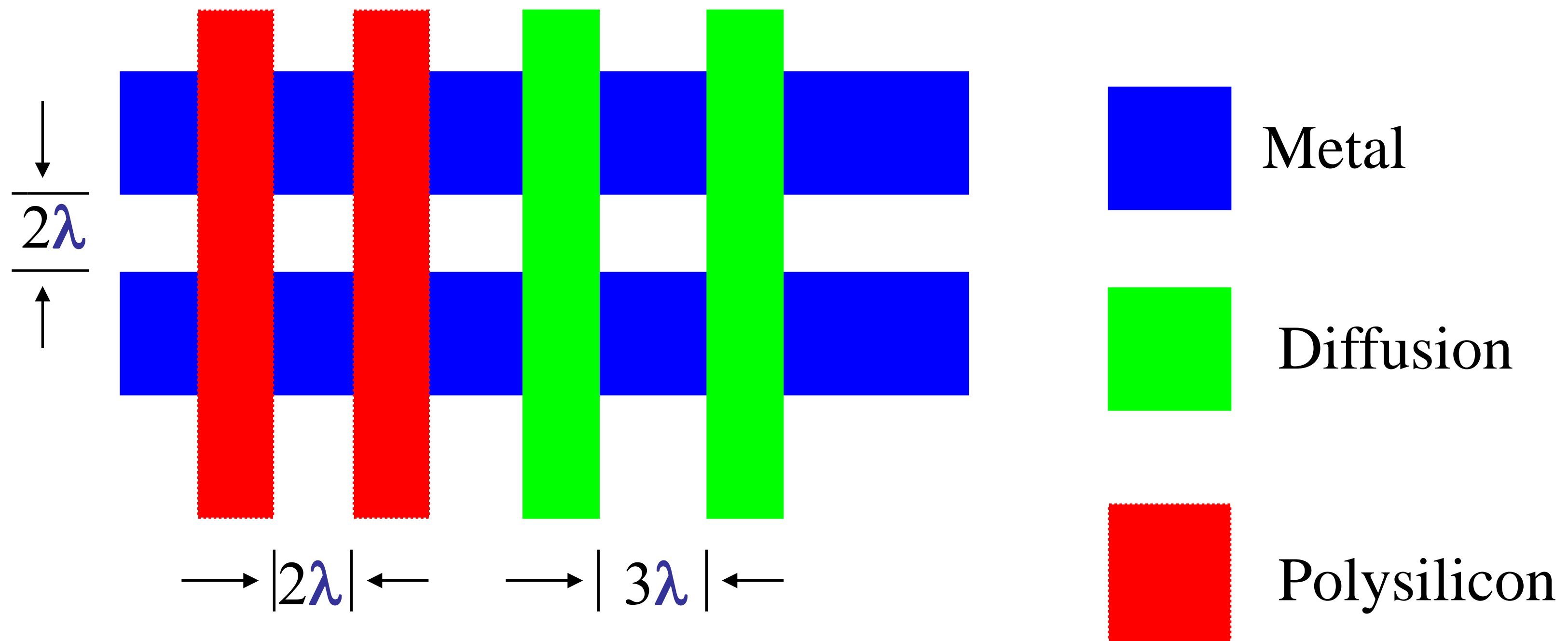
DESIGN RULES

- Minimum width of PolySi and diffusion line **2λ**
- Minimum width of Metal line **3λ** as metal lines run over a more uneven surface than other conducting layers to ensure their continuity



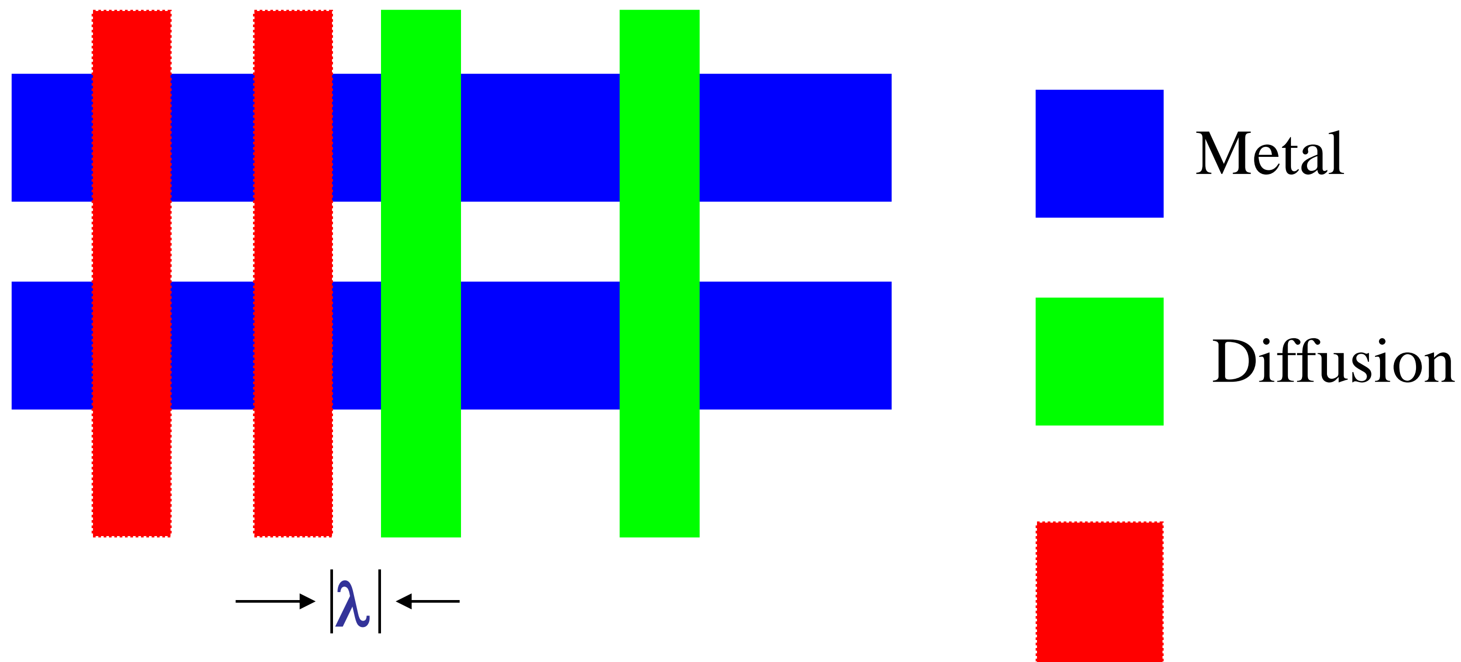
DESIGN RULES

- **PolySi – PolySi space 2λ**
- **Metal - Metal space 2λ**
- **Diffusion – Diffusion space 3λ To avoid the possibility of their associated regions overlapping and conducting current**



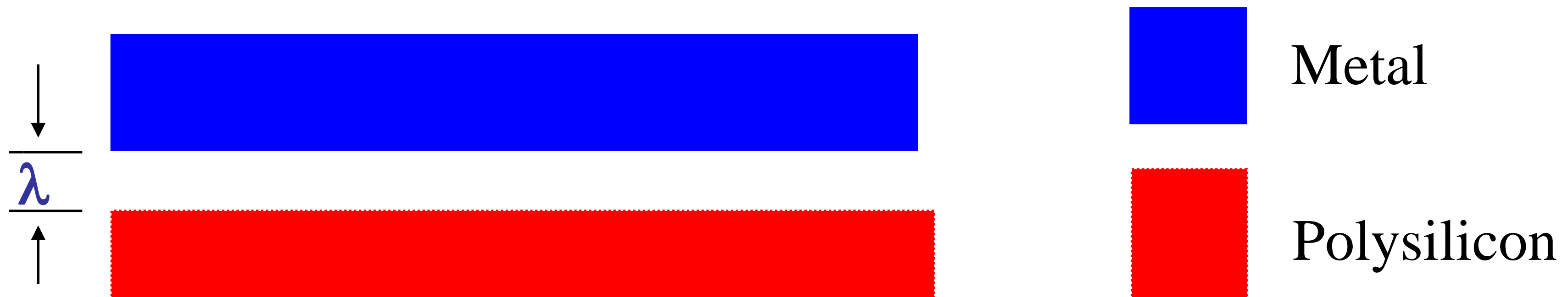
DESIGN RULES

- **Diffusion – PolySi space λ To prevent the lines overlapping to form unwanted capacitor**
- **Metal lines can pass over both diffusion and polySi without electrical effect. Where no separation is specified, metal lines can overlap or cross**



DESIGN RULES

- **Metal lines can pass over both diffusion and polySi without electrical effect**
- **It is recommended practice to leave λ between a metal edge and a polySi or diffusion line to which it is not electrically connected**



- **Recall**
  - **poly-poly spacing 2λ**
  - **diff-diff spacing 3λ (depletion regions tend to spread outward)**
  - **metal-metal spacing 2λ**
  - **diff-poly spacing λ**

Butting Contact

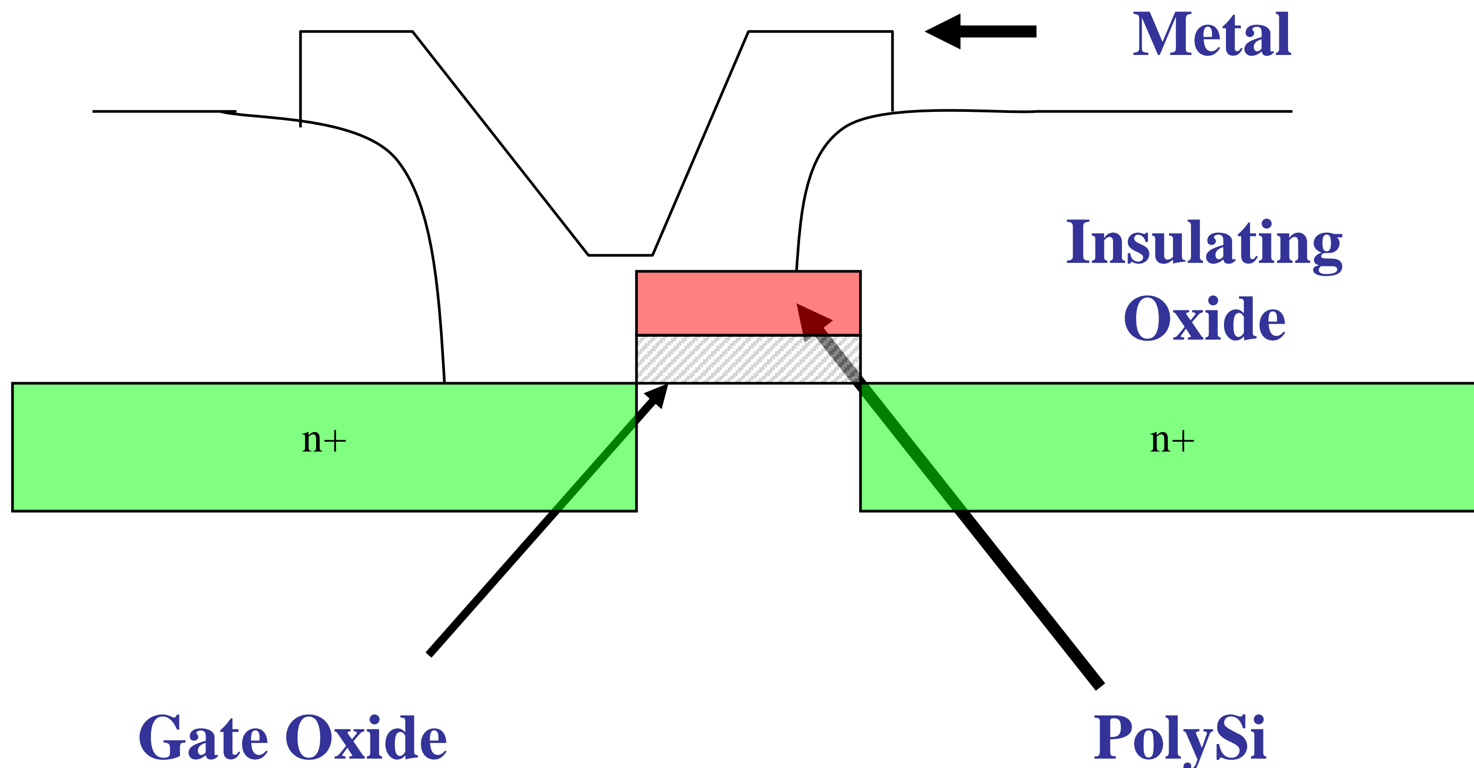
The gate and source of a depletion device can be connected by a method known as **butting contact.** Here metal makes contact to both the diffusion forming the source of the depletion transistor and to the polySi forming this device's gate.

Advantage:

No buried contact mask required and avoids associated processing.

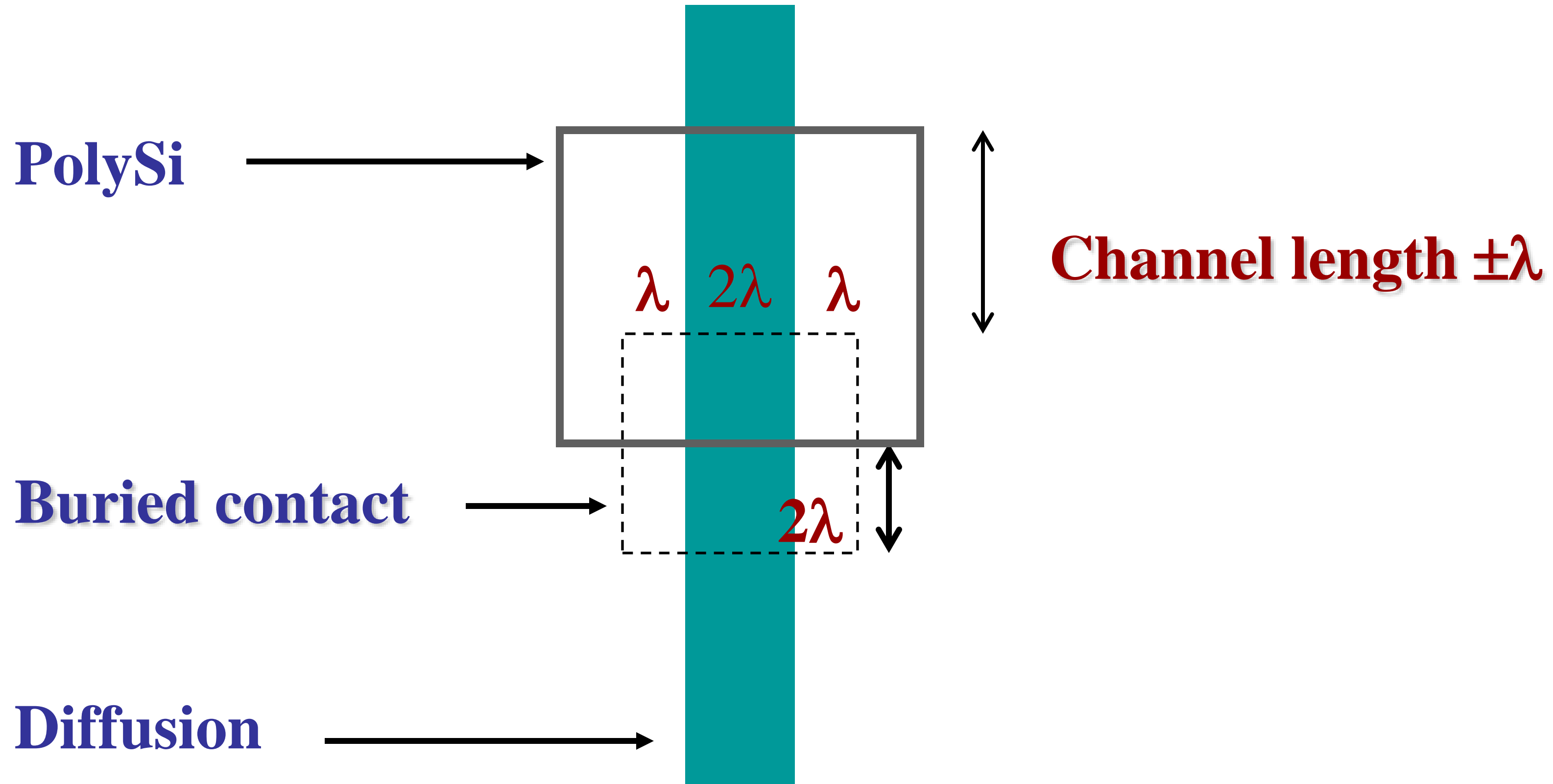
Butting Contact

Problem: **Metal descending the hole has a tendency to fracture at the polySi corner, causing an open circuit.**



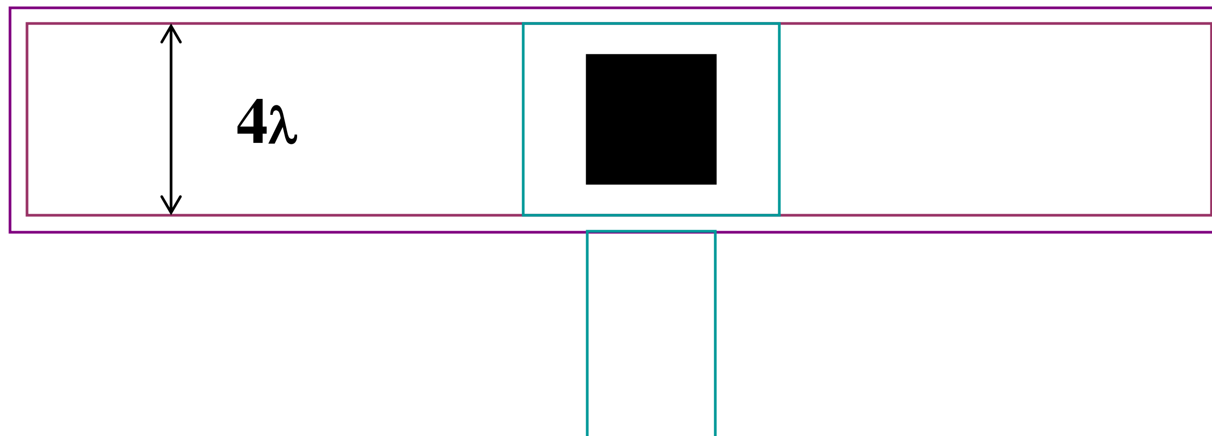
Buried Contact

Here gate length is depend upon the alignment of the buried contact mask relative to the polySi and therefore vary by ±λ.



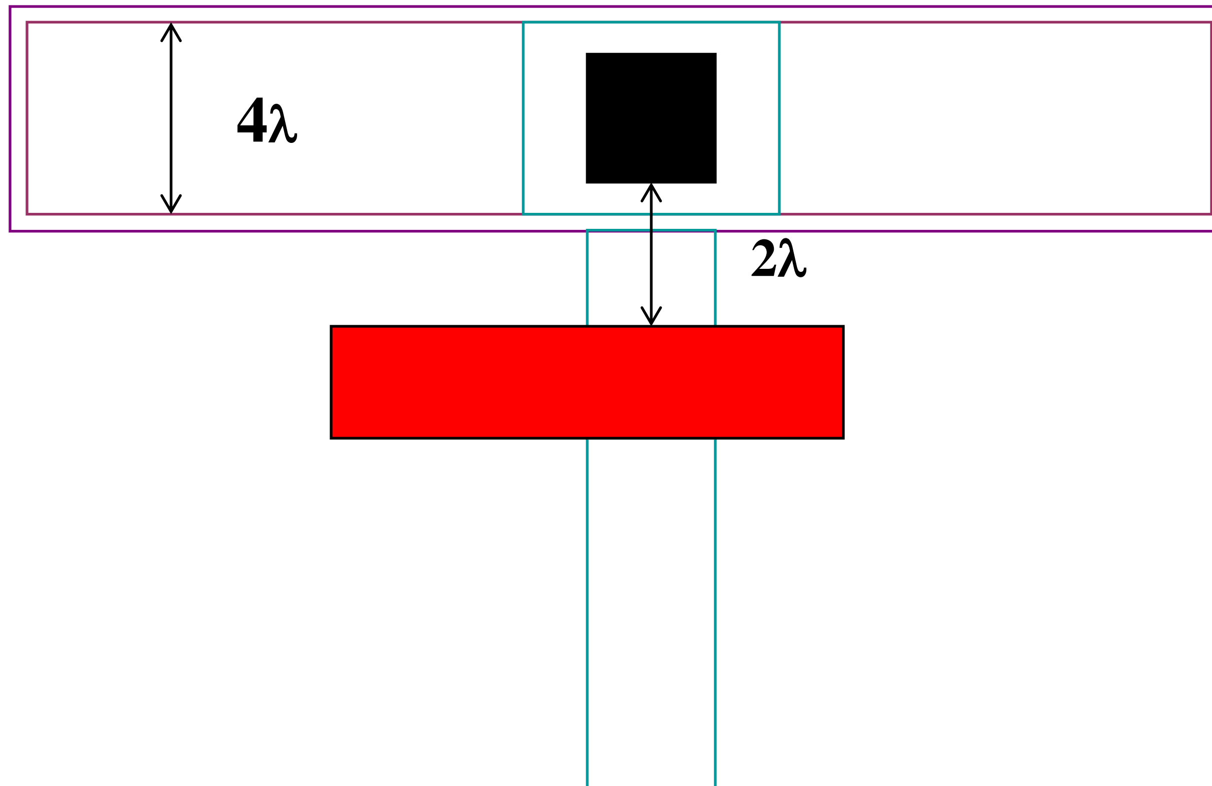
Contact Cut

- **Metal connects to polySi/diffusion by contact cut.**
- **Contact area: 2 λ X 2 λ**
- **Metal and polySi or diffusion must overlap this contact area by l so that the two desired conductors encompass the contact area despite any mis-alignment between conducting layers and the contact hole**



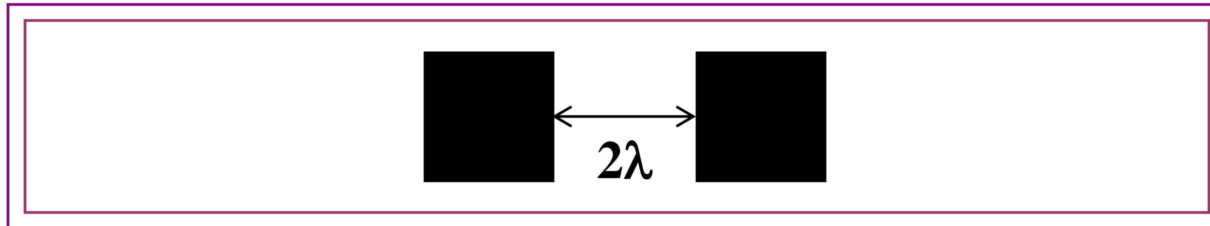
Contact Cut

- **Contact cut – any gate: 2 λ apart**
- **Why? No contact to any part of the gate.**

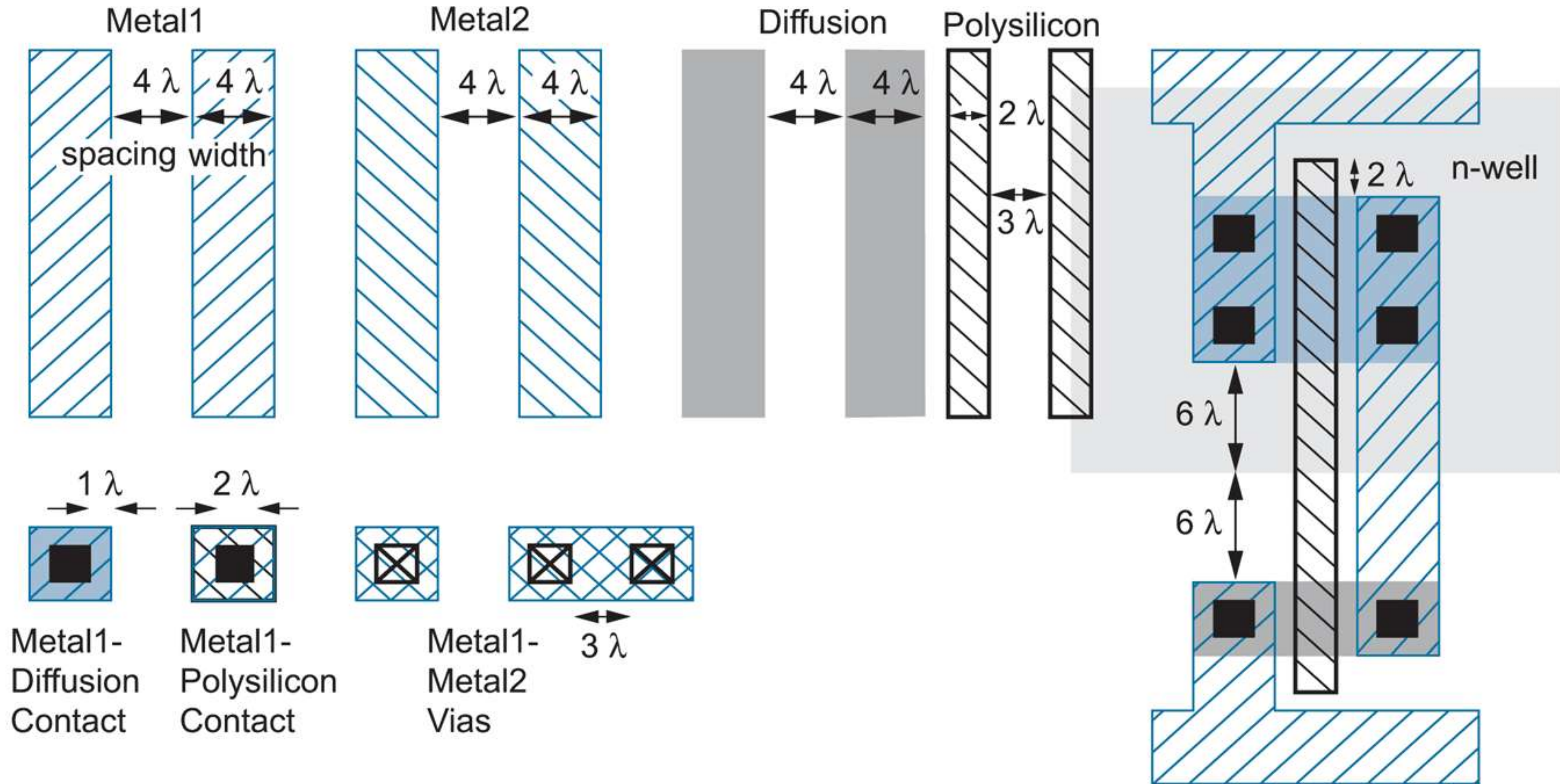


Contact Cut

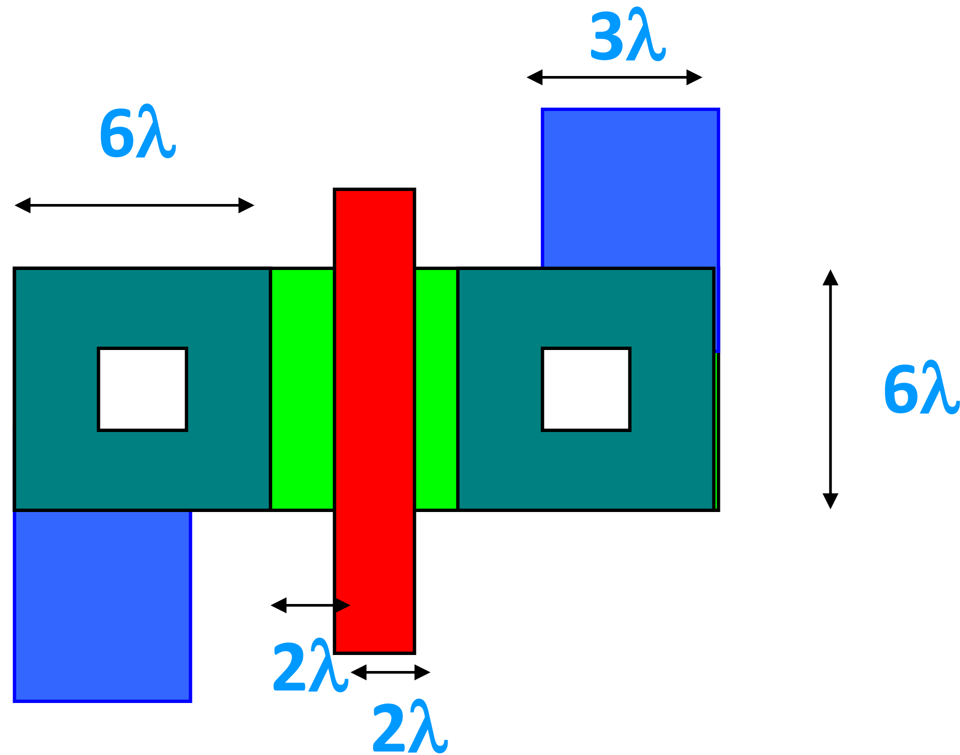
- **Contact cut – contact cut: 2 λ apart**
- **Why? To prevent holes from merging.**



DESIGN RULES

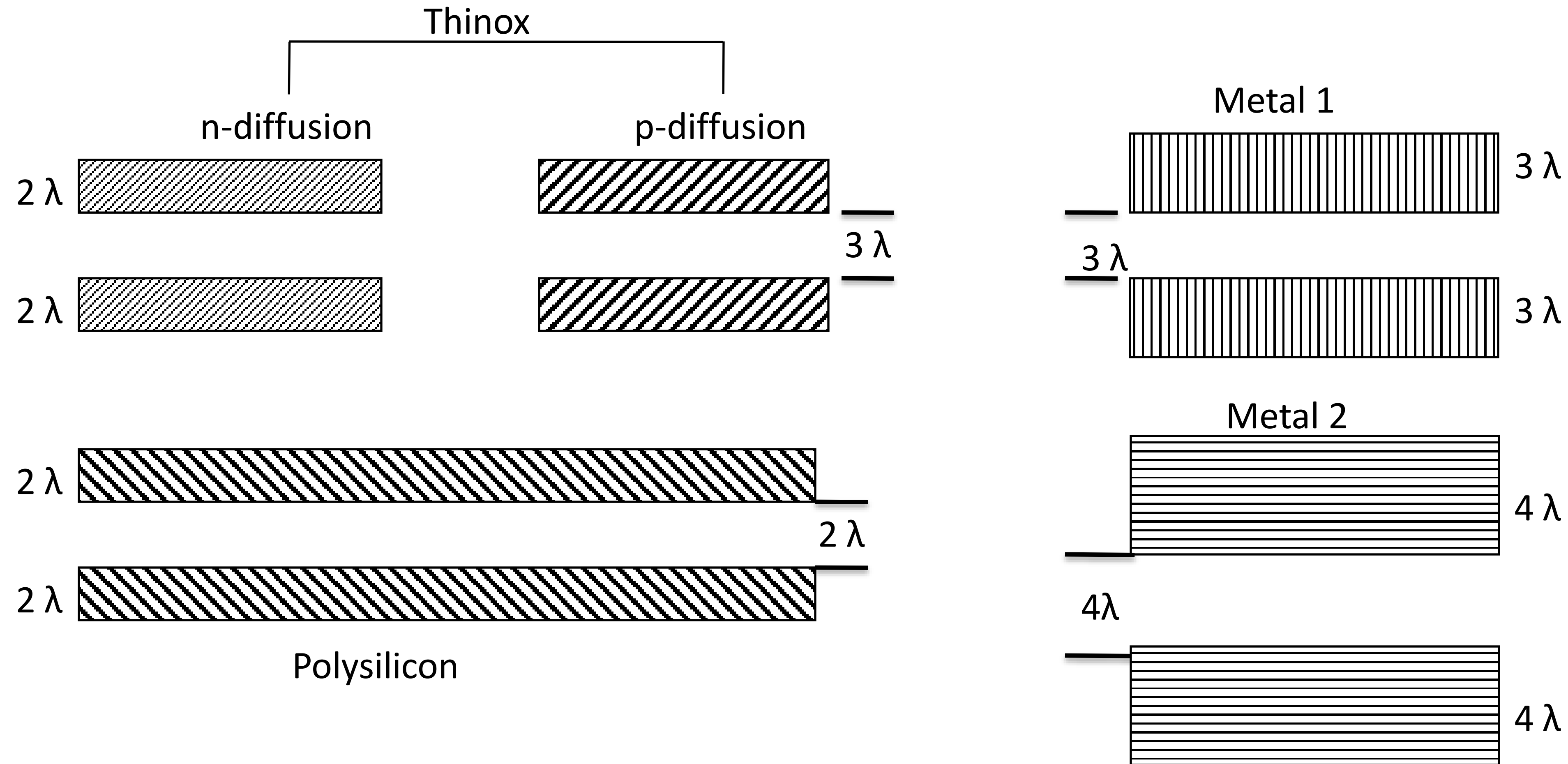


DESIGN RULES

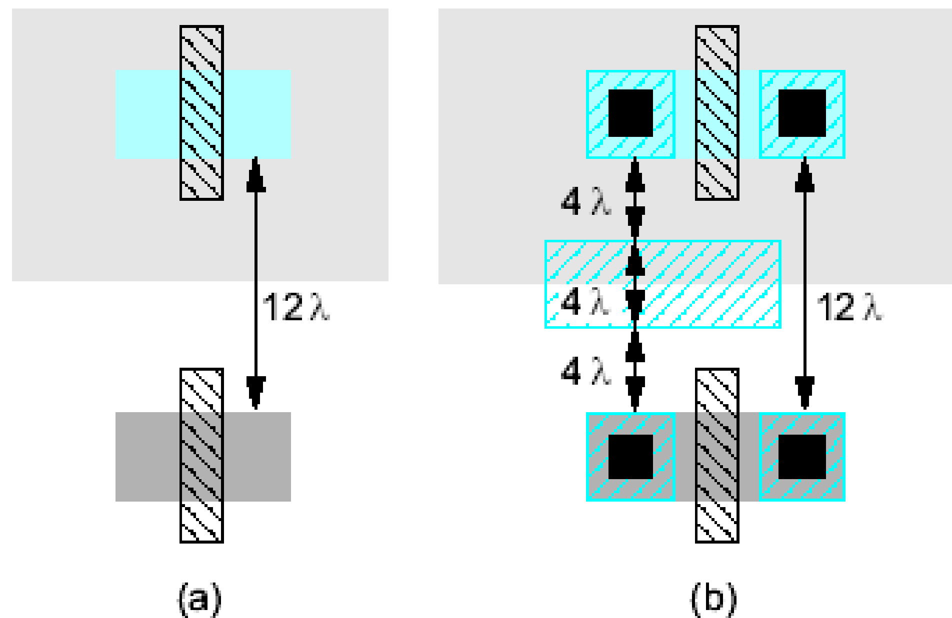


All device mask dimensions are based on multiples of λ, e.g., polysilicon minimum width = 2λ. Minimum metal to metal spacing = 3λ

DESIGN RULES

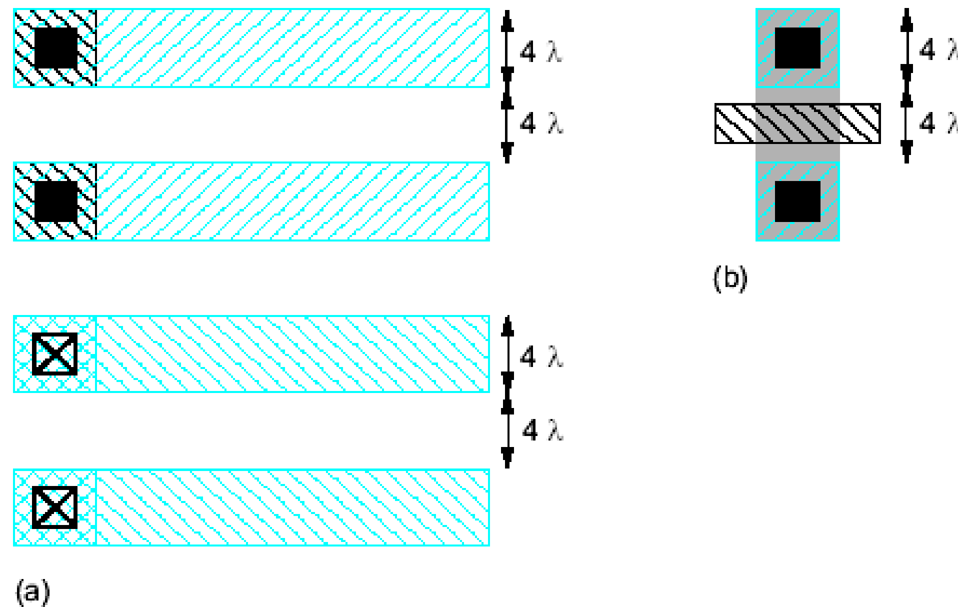


- Wells must surround transistors by 6 λ
  - Implies 12 λ between opposite transistor flavors
  - Leaves room for one wire track



DESIGN RULES

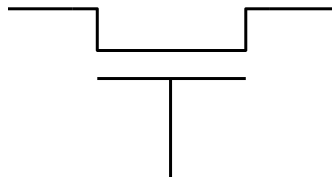
- A *wiring track* is the space required for a wire
  - 4 λ width, 4 λ spacing from neighbour = 8 λ pitch
- Transistors also consume one wiring track

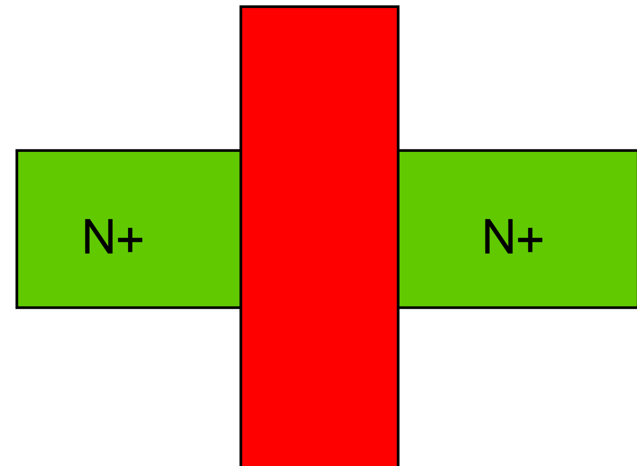


LAYOUTS

- **Layer Types**
  - p-substrate
  - n-well
  - n+
  - p+
  - Gate oxide
  - Gate (polysilicon)
  - Field Oxide
    - Insulated glass
    - Provide electrical isolation

LAYOUTS





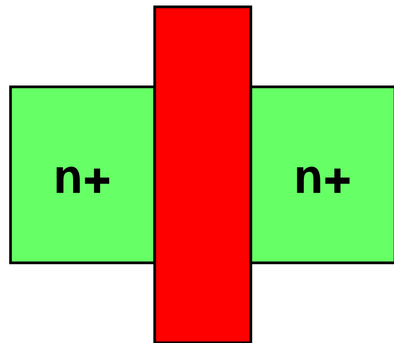
Top view of the FET pattern

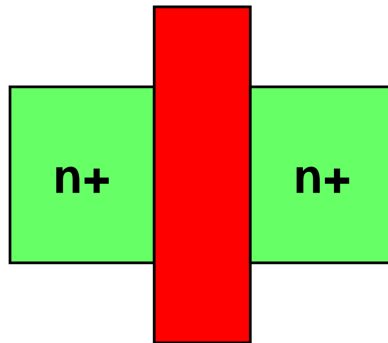
NMOS

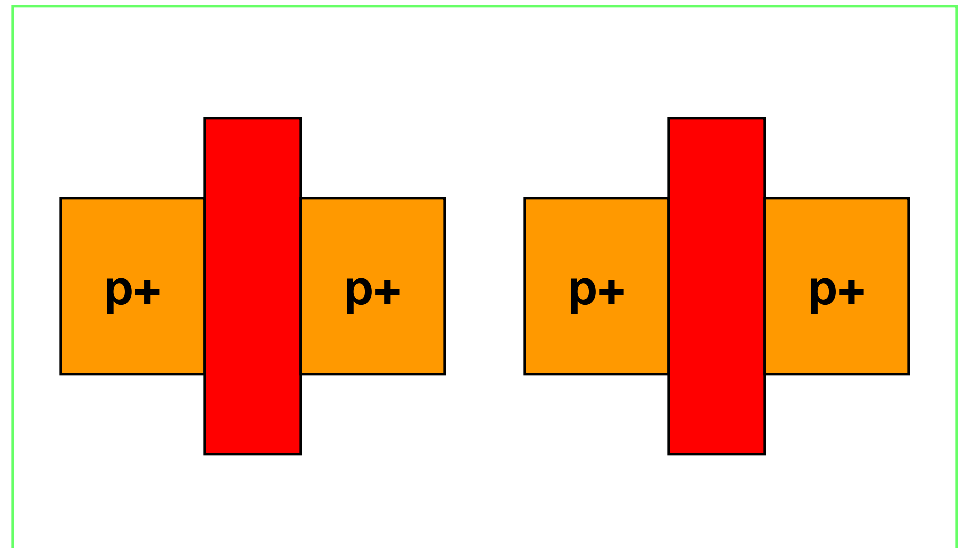
NMOS

PMOS

PMOS

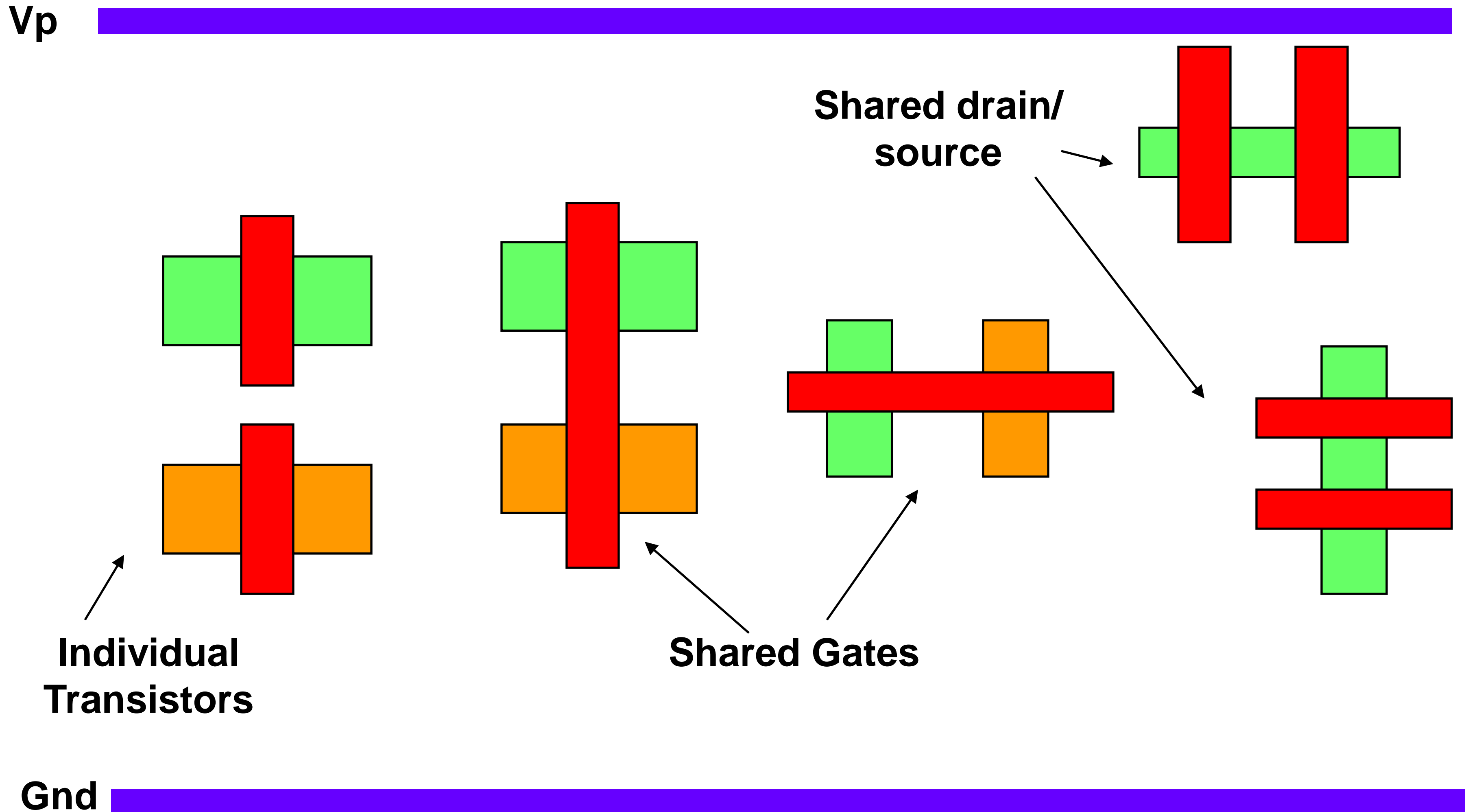






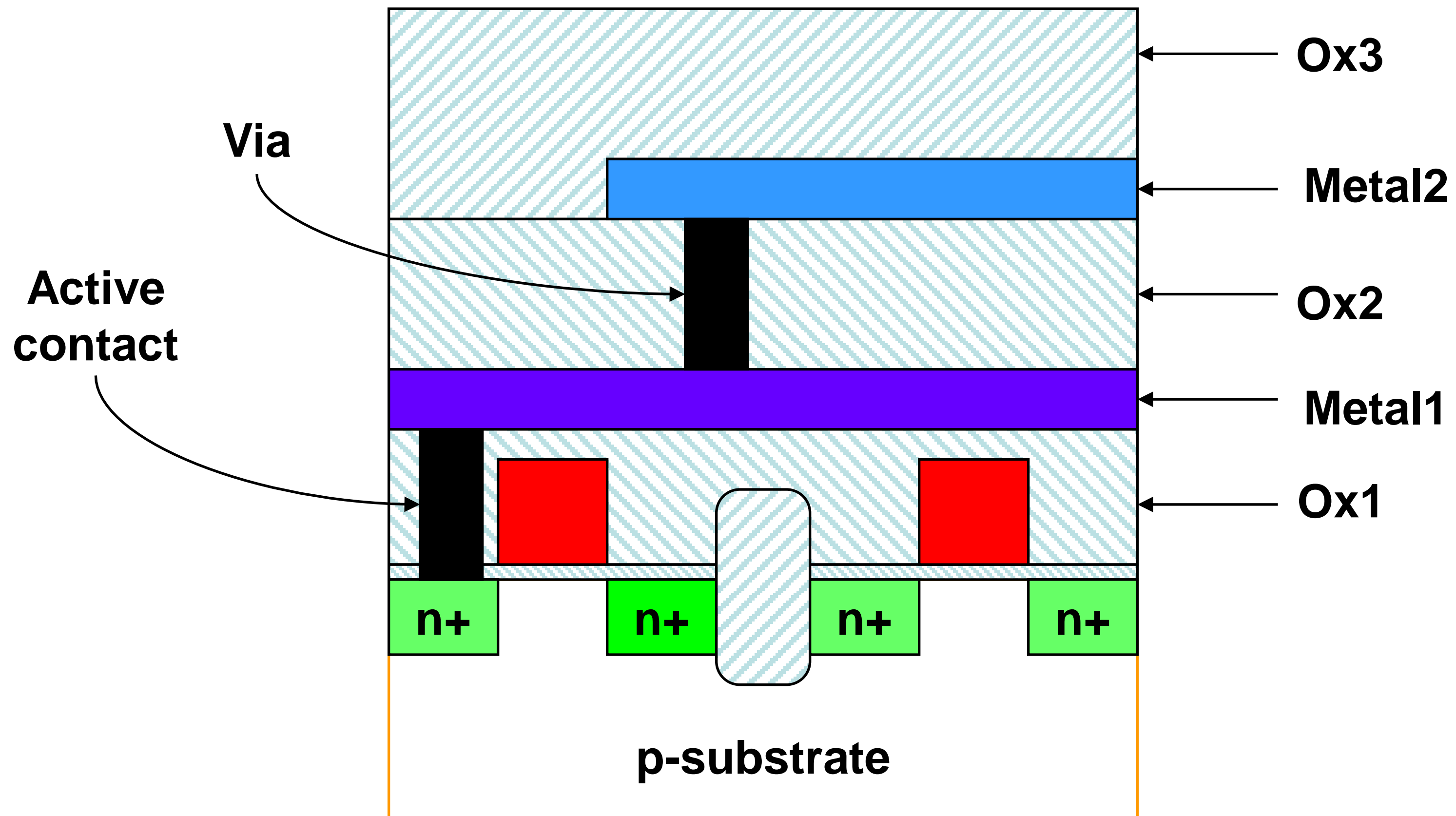
n-well

General Layout Geometry

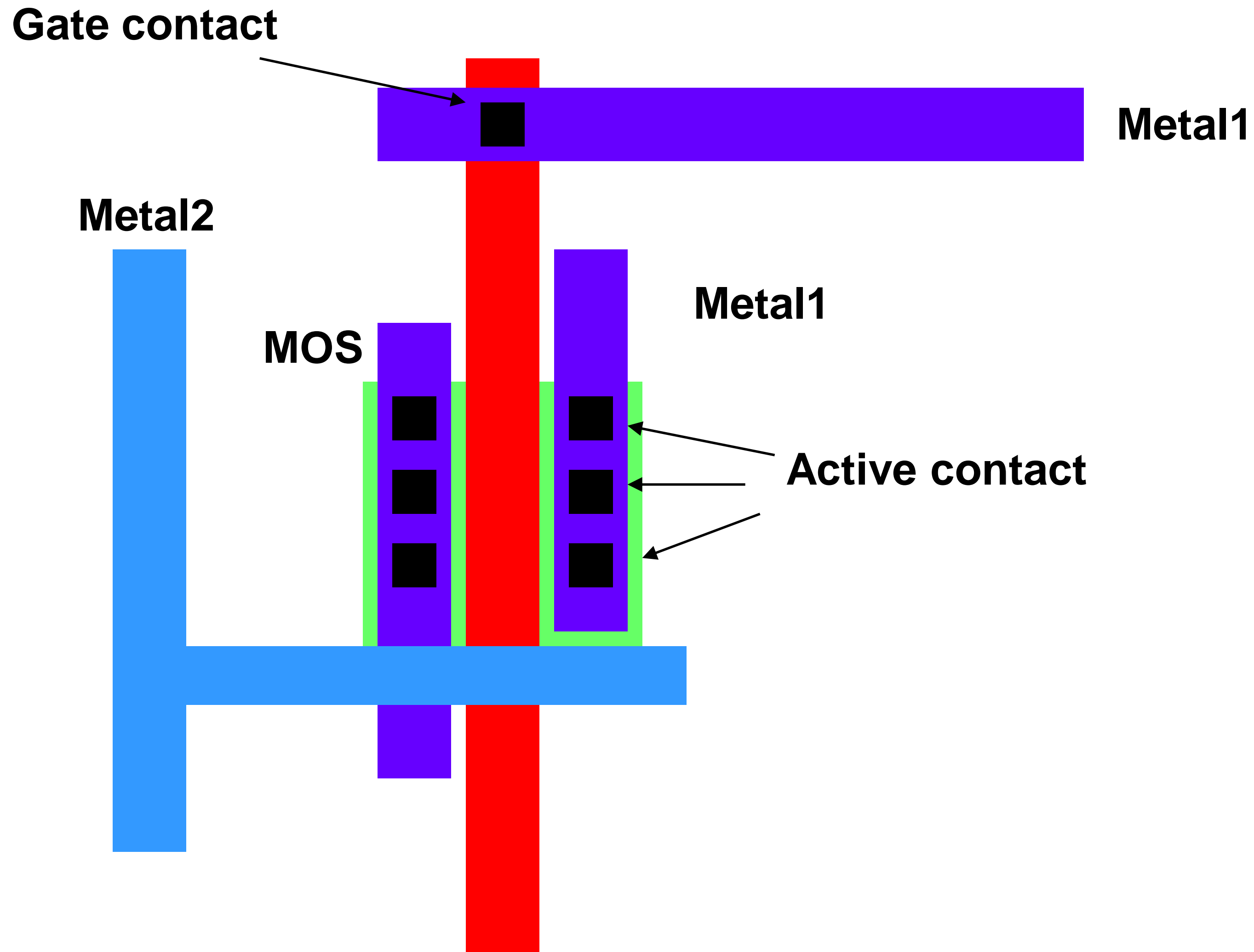


Metal Interconnect Layers

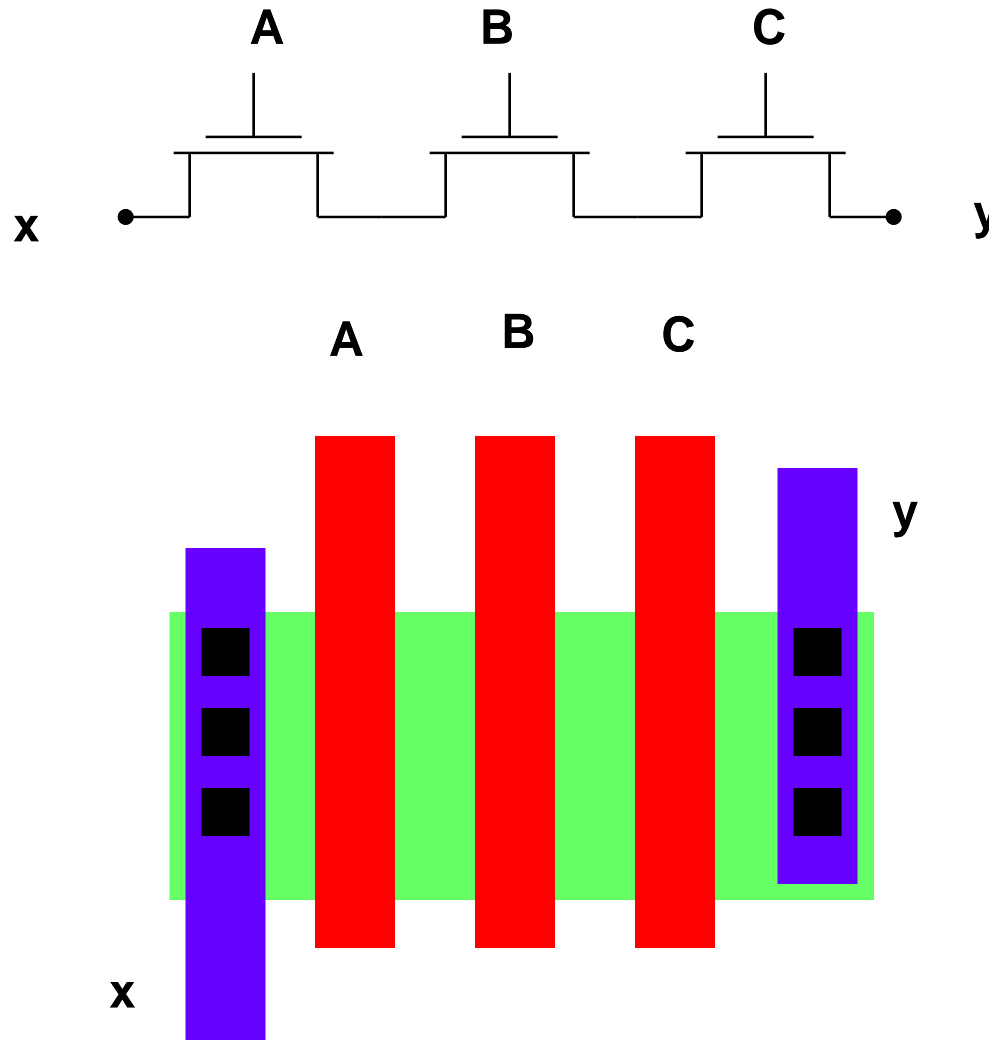
- Metal layers are electrically isolated from each other
- Electrical contact between adjacent conducting layers requires contact cuts and vias



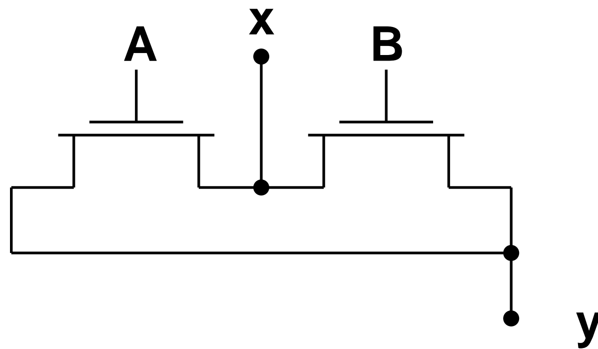
Interconnect Layout Example

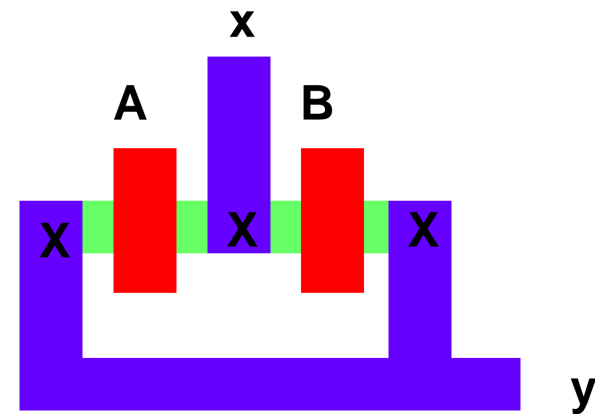


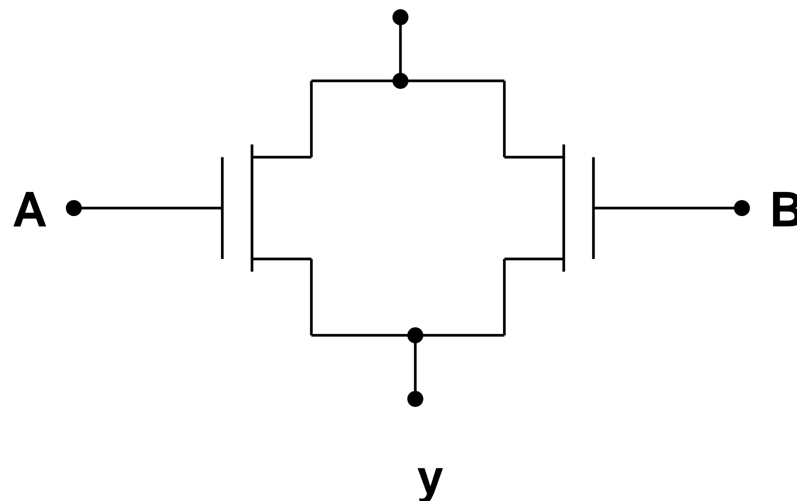
Designing MOS Arrays

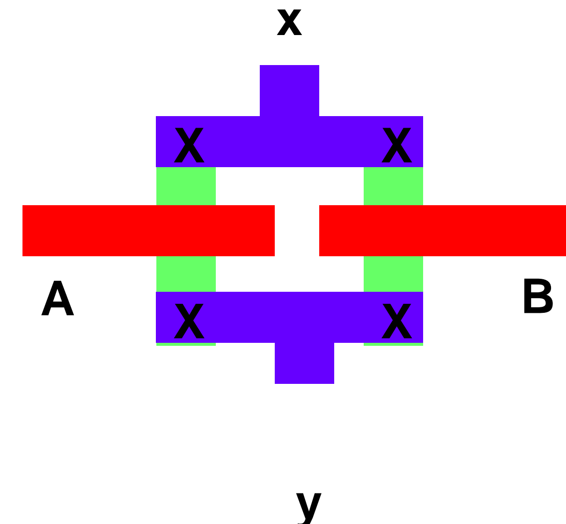


Parallel Connected MOS Patterning





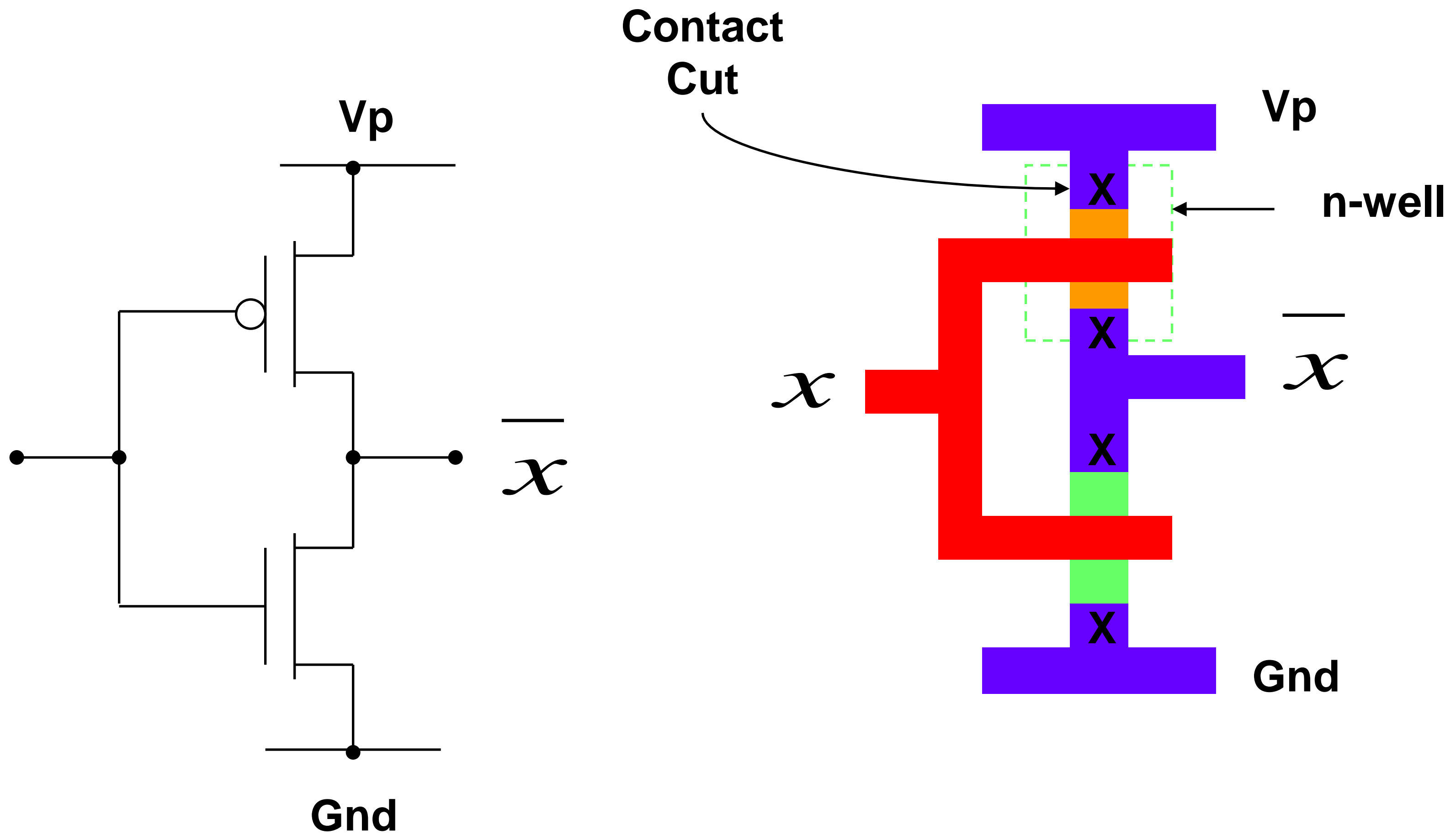




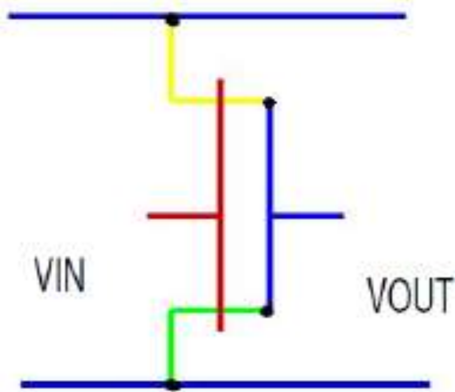
Basic Gate Design

- Both the power supply and ground are routed using the Metal layer
- n+ and p+ regions are denoted using the same fill pattern. The only difference is the n-well
- Contacts are needed from Metal to n+ or p+

The CMOS NOT Gate



The CMOS NOT Gate



Substrate contact

Vdd

nwell

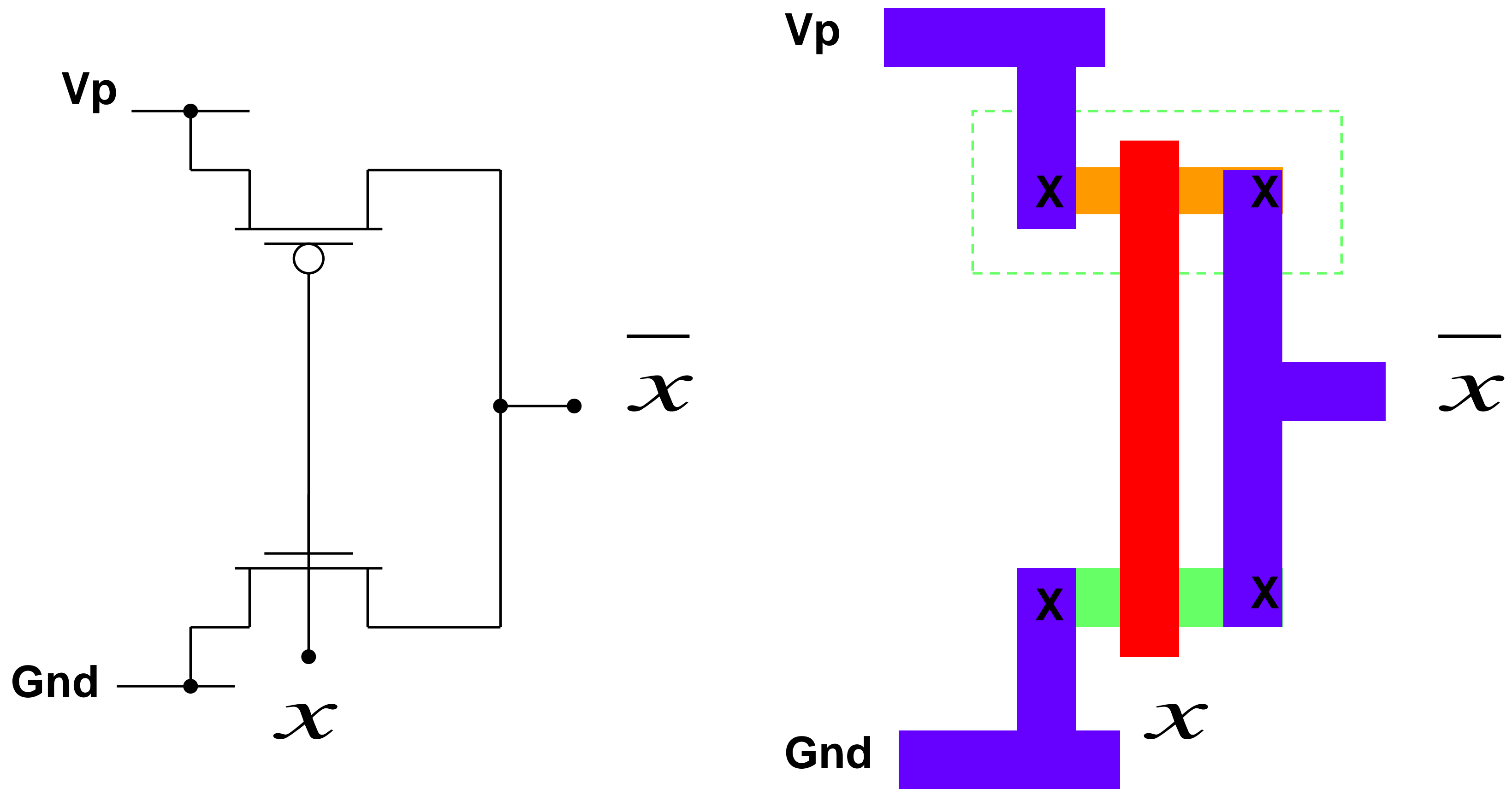
Vin

Vout

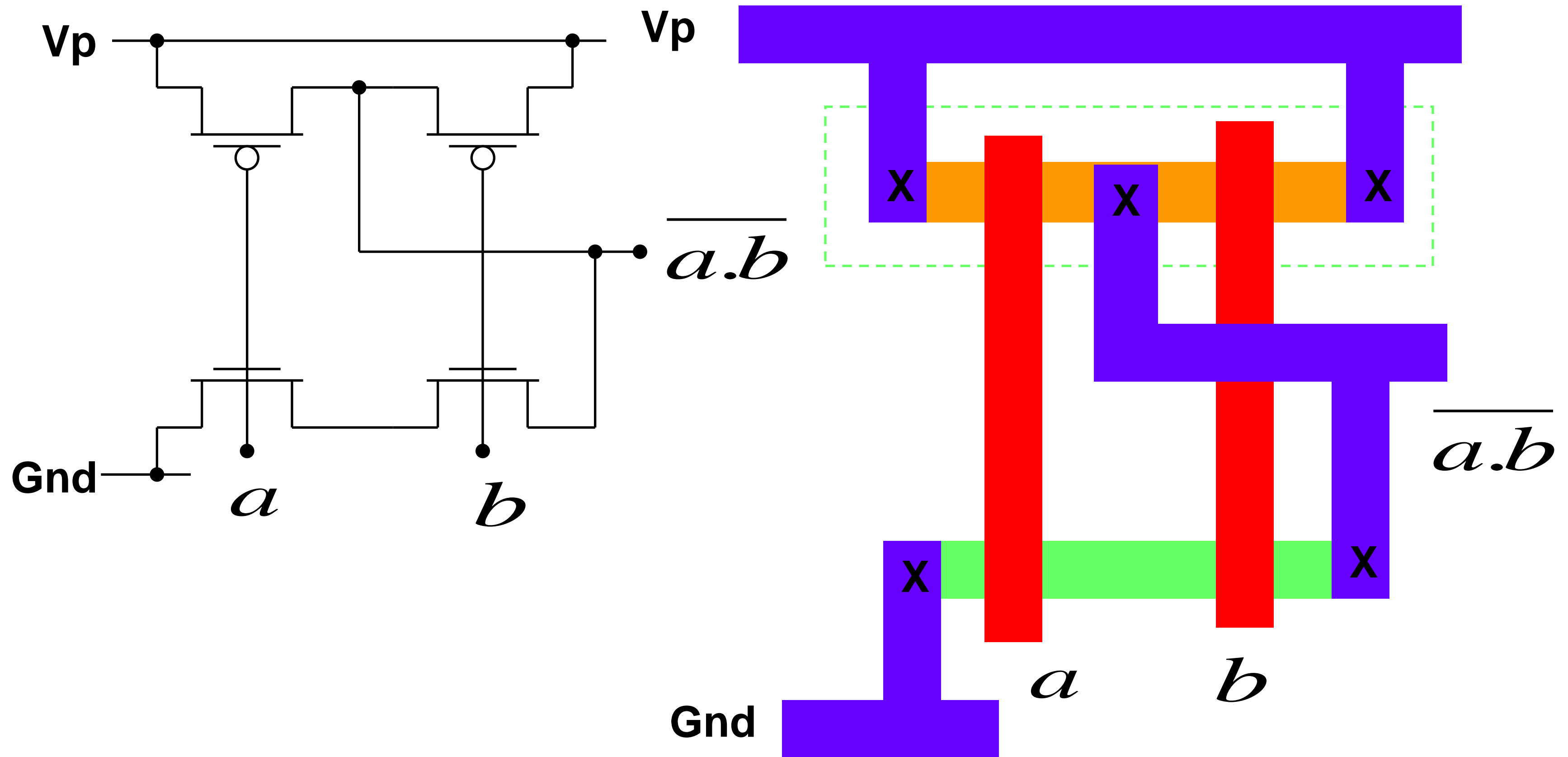
Substrate contact

Vss

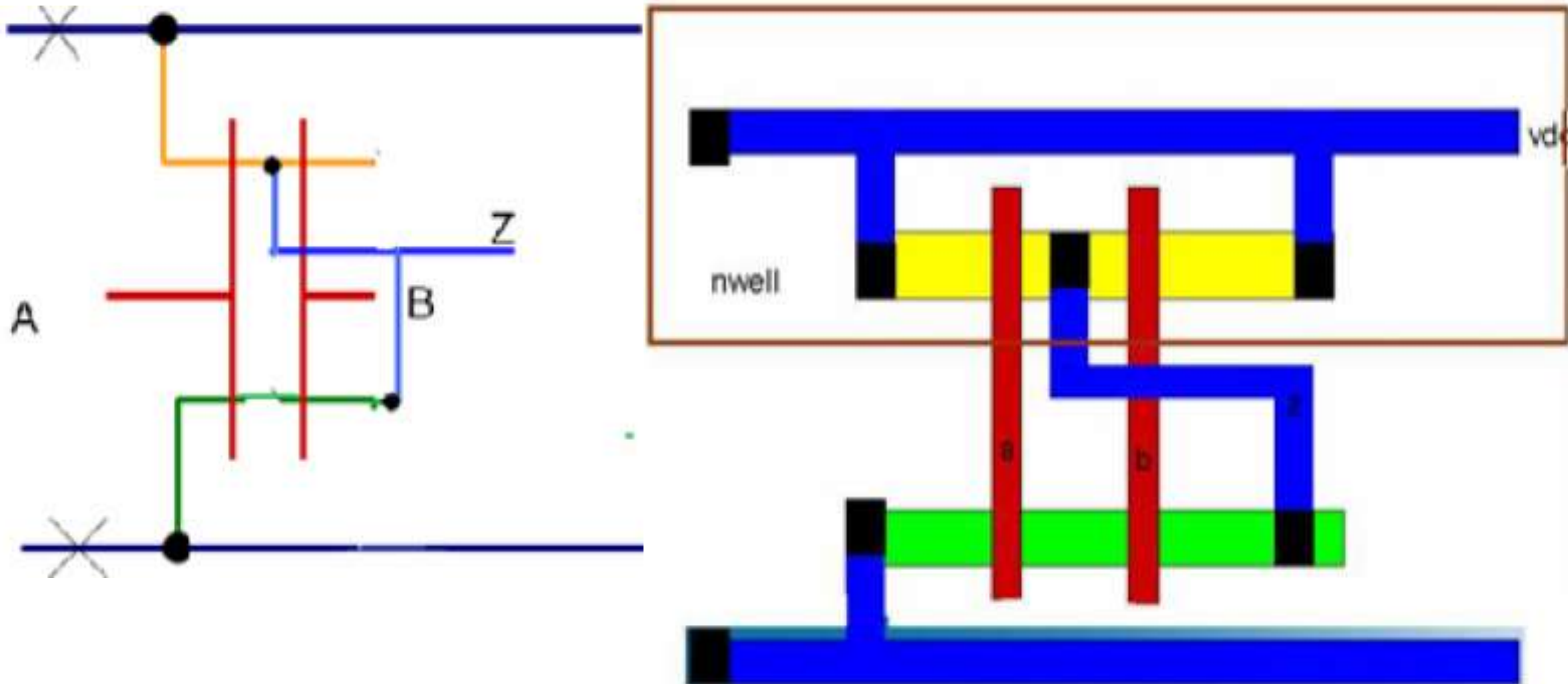
The CMOS NOT Gate



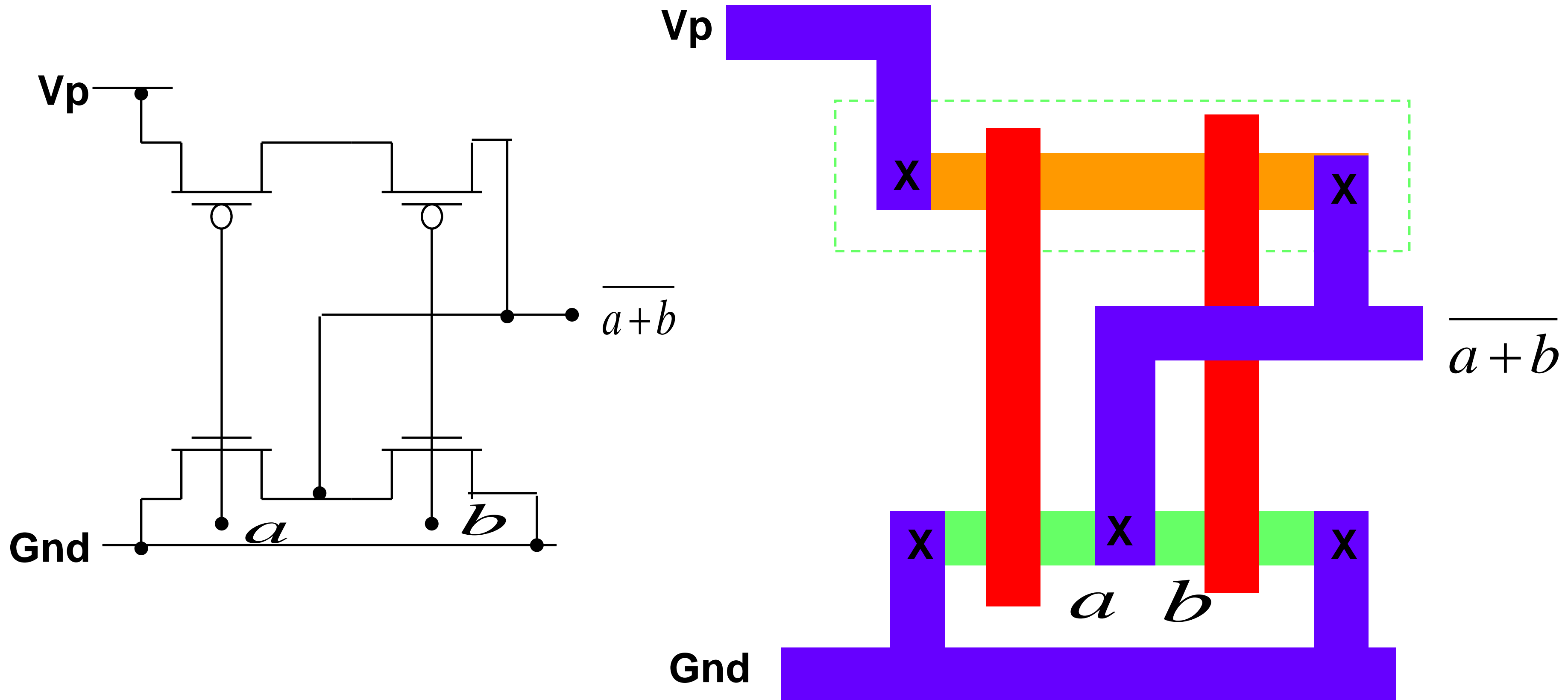
The CMOS NAND Gate



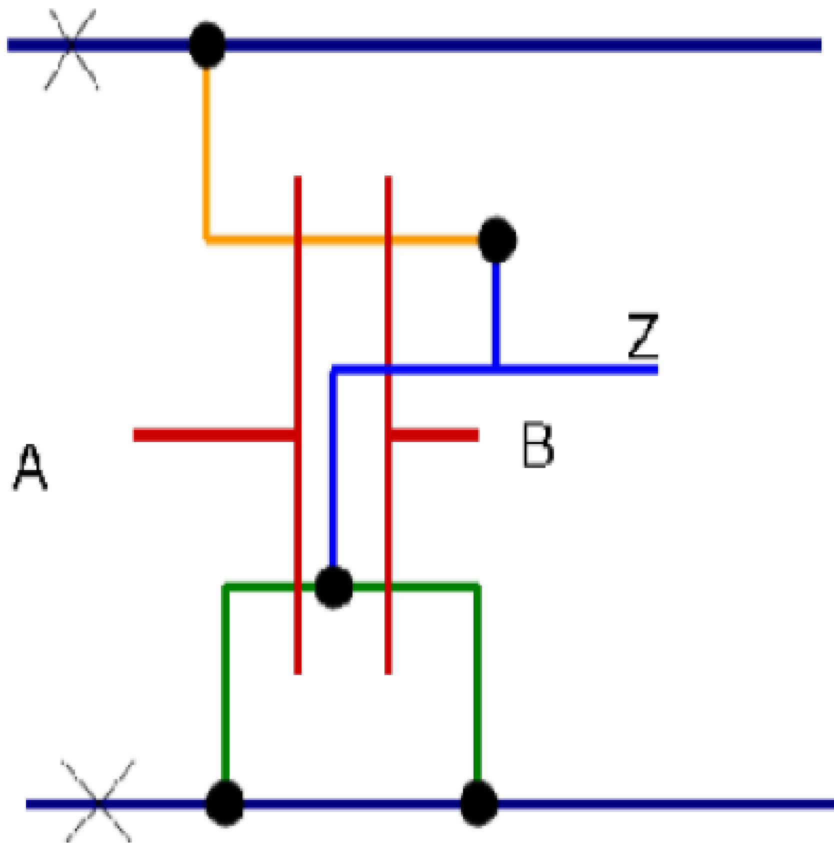
The CMOS NAND Gate

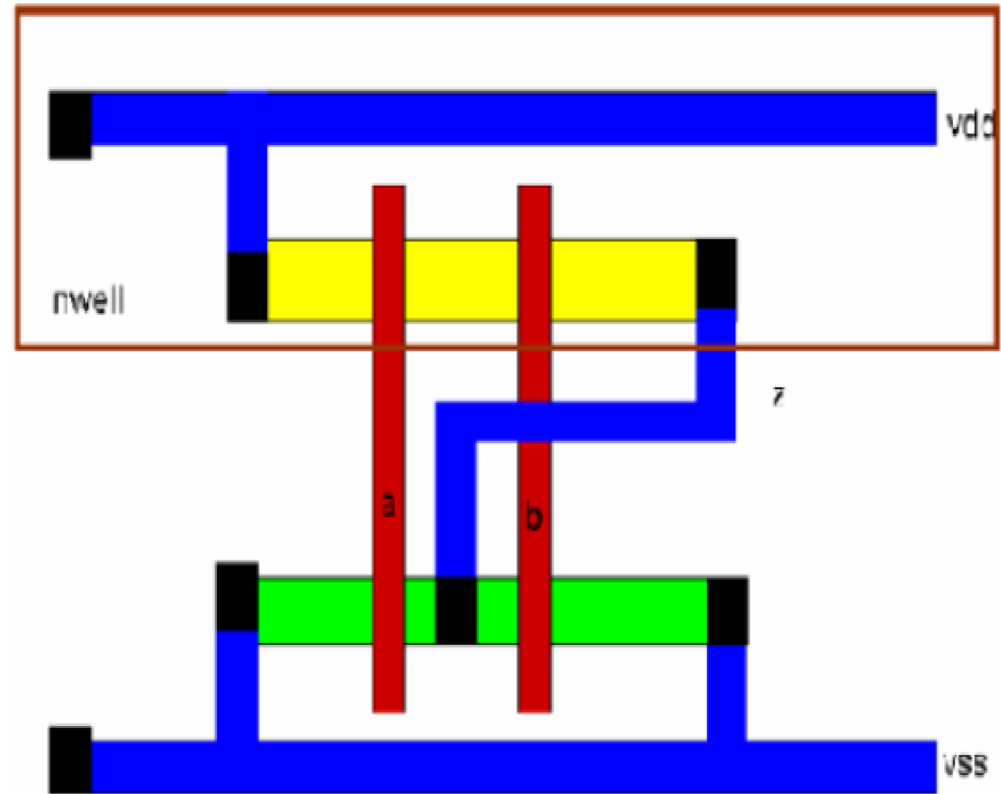


The CMOS NOR Gate

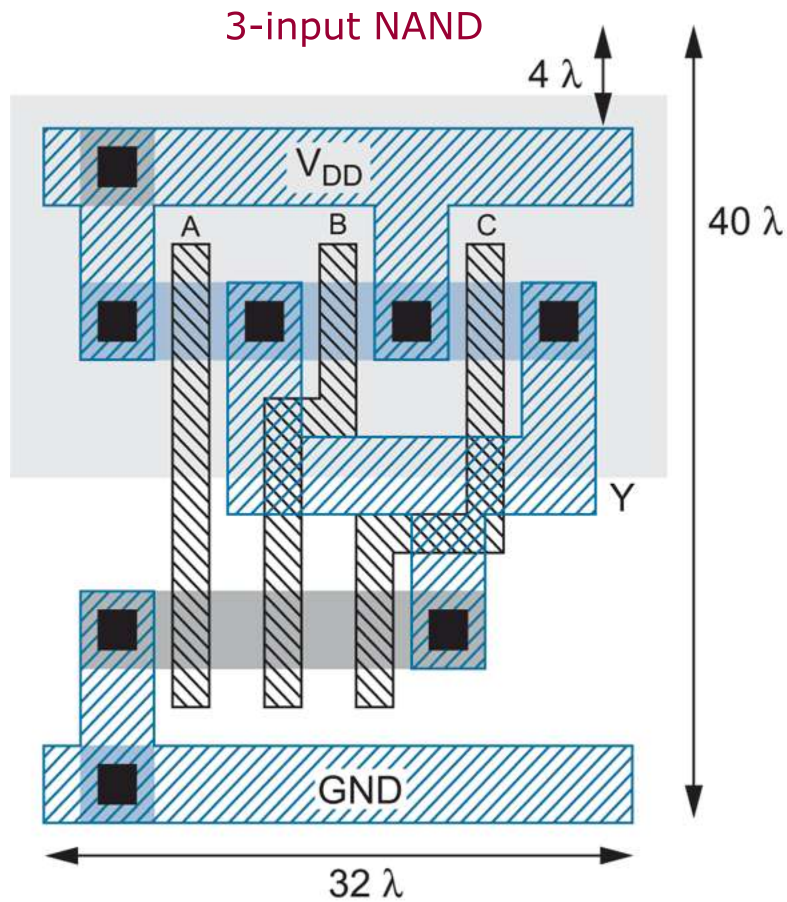


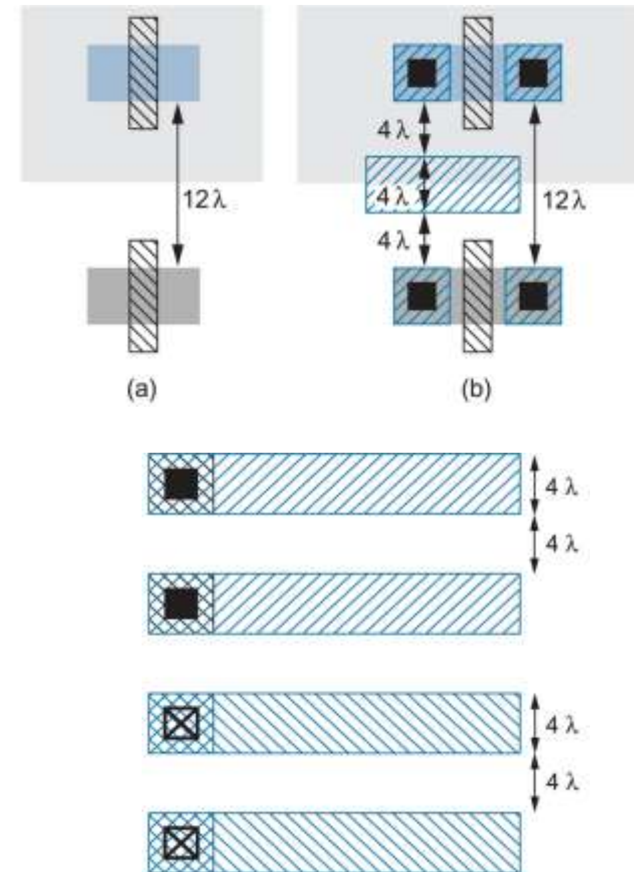
The CMOS NOR Gate



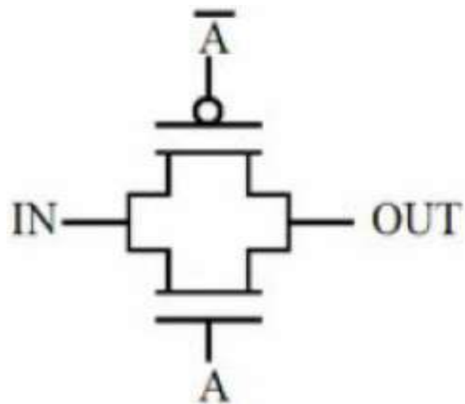


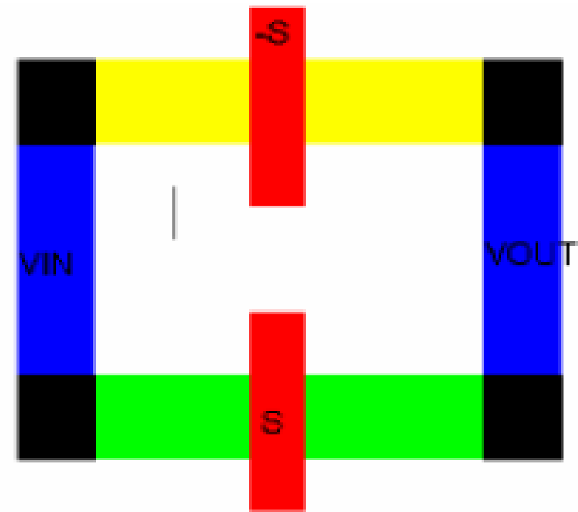
The 3-Input NAND Gate



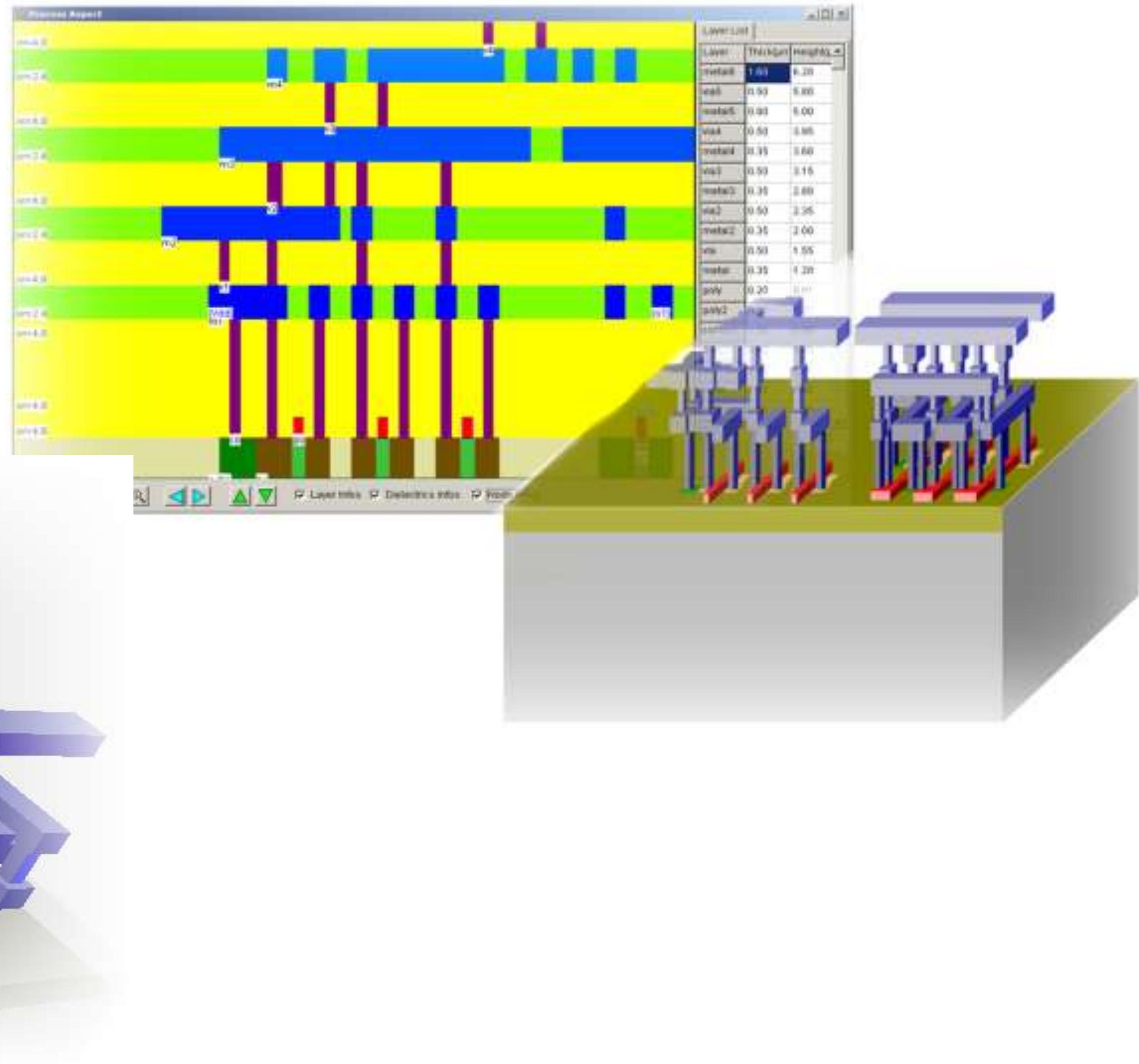


The Transmission Gate





The 3-D View of a Design



GENERAL LAYOUT GUIDELINES

1. The electrical gate design must be completed by checking the followings:
   a. Right power and ground supplies
   b. Noise at the gate input
   c. Faulty connections and transistors
   d. Improper ratios
   e. Incorrect clocking and charge sharing
2. V_{DD} and the V_{SS} lines run at the top and the bottom of the design
3. Vertical poysilicon for each gate input
4. Order polysilicon gate signals for maximal connection between transistors
5. The connectivity requires to place NMOS close to V_{SS} and PMOS close to V_{DD}
6. Connection to complete the logic must be made using poly, metal and even metal2

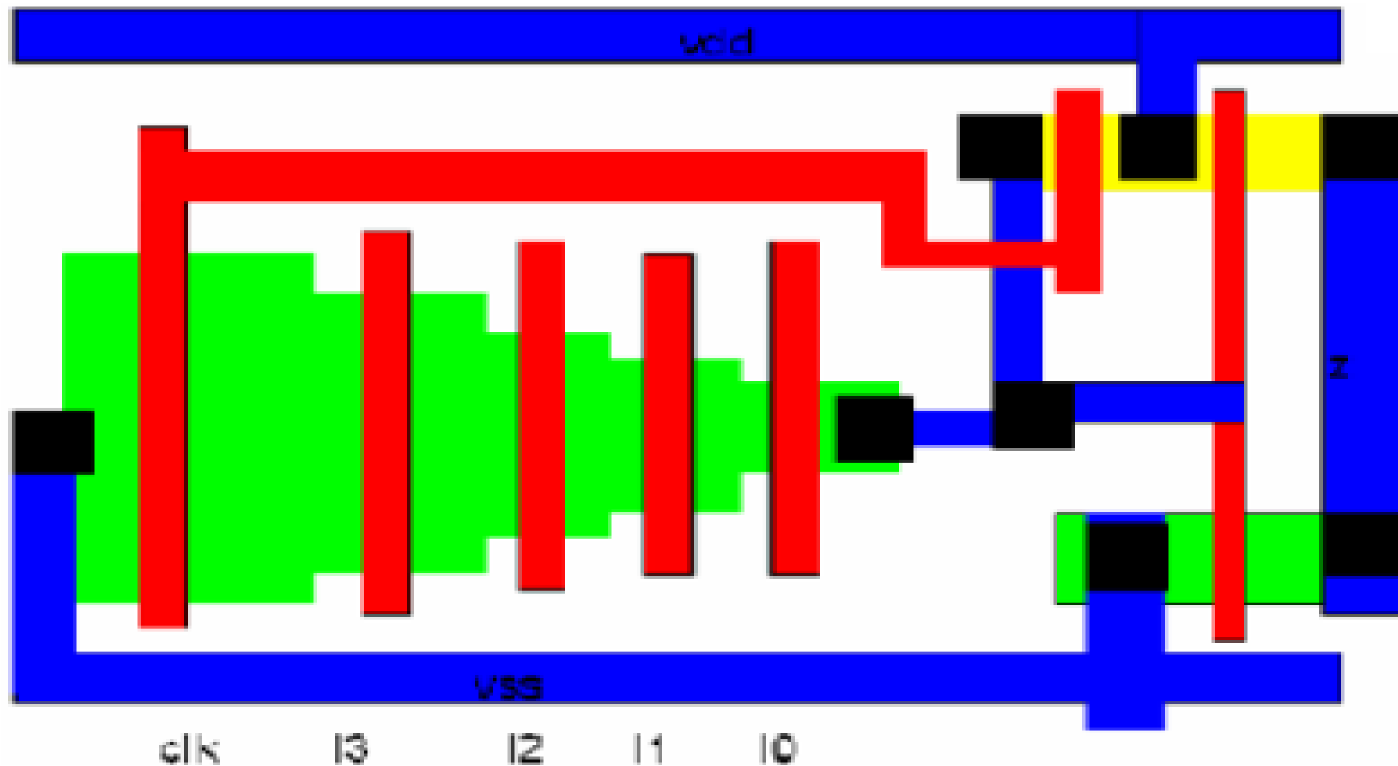
GENERAL LAYOUT GUIDELINES

The factors for density improvement are (optimization):

- Efficient routing space usage. They can be placed over the cells or even in multiple layers.
- Source drain connections must be merged better.
- White (blank) spaces must be minimum.
- The devices must be of optimum sizes.
- Transparent routing can be provided for cell to cell interconnection, this reduces global wiring problems

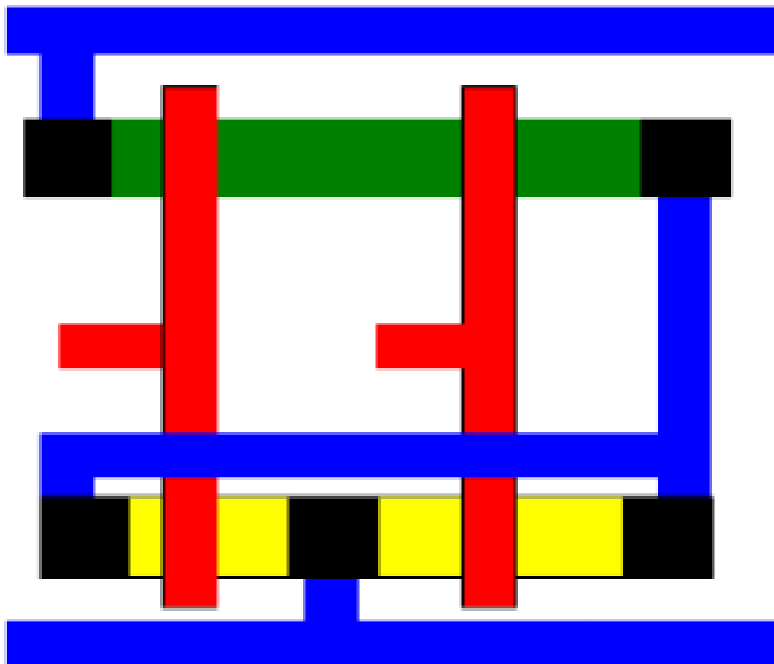
LAYOUT OPTIMIZATION FOR PERFORMANCE

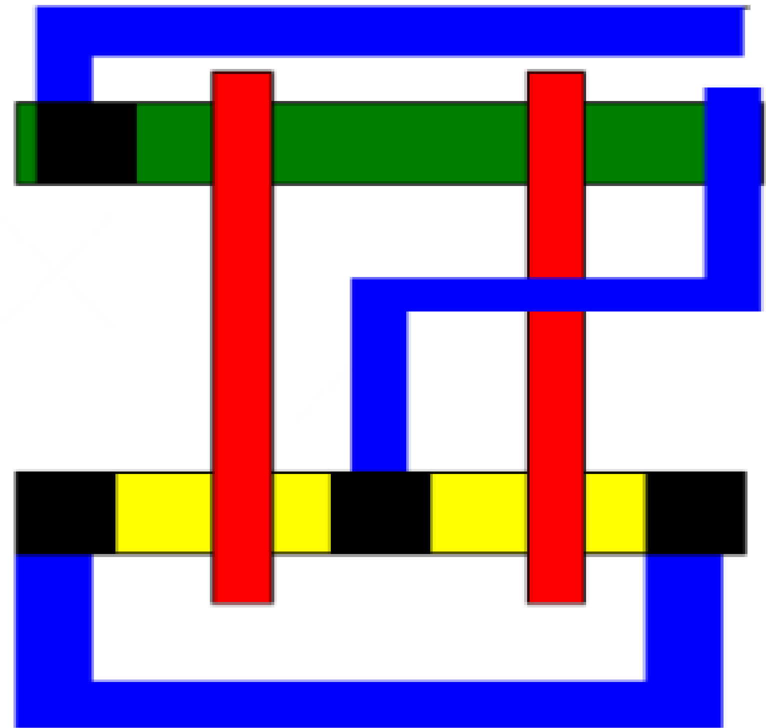
1. Vary the size of the transistor according to its position in series. The transistor closest to the output is the smallest. The transistor nearest to the VSS line is the largest. This helps in increasing the performance by 30%. A three input NAND gate with the varying size is shown.



LAYOUT OPTIMIZATION FOR PERFORMANCE

1. When drains are connected in parallel, must try and reduce the number of drains in parallel i.e. wherever possible must try and connect drains in series at least at the output. This arrangement could reduce the capacitance at the output enabling good voltage levels.





BASIC PHYSICAL DESIGN

The VLSI design flow for any IC design is as follows

1. Specification (problem definition)
2. Schematic (gate level design) (equivalence check)
3. Layout (equivalence check)
4. Floor Planning
5. Routing, Placement
6. On to Silicon

ANY Qs?